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Harmonic Mitigation

Work Package Two – Algorithm design, development and implementation for single inverter control

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Glossary

Abbreviation	Term
AF	Active Filter
BSP	Bulk Supply Point
CB	Circuit Breaker
EMT	Electromagnetic transient
FD	Frequency distribution
FFT	Fast Fourier Transformation
PI	Proportional integral
PCC	Point of common coupling
PLL	Phase locked-loop
PR	Proportional resonant
PWM	Pulse-width modulation
Rms	Root mean square
SCADA	Supervisory control and data acquisition
THD	Total harmonic distortion
WPD	Western Power Distribution

Work Package Summary

The work reported here describes Work Package 2 (WP2) of the WPD NIA Harmonic Mitigation project: the development and validation of a control algorithm to provide existing PV inverters with active filter (AF) functionality. The AF functionality is in addition to the main task performed by these devices, i.e. the delivery of power from the photovoltaic panels to the power grid.

The chosen modelling environment for this work is MATLAB/Simulink. A detailed model of the PV inverters and power system under consideration has been built and validated as part of Work Package 1 (WP1). The harmonic mitigation algorithm was iteratively developed and tested within this modelling environment, and the resulting impact of operating the algorithm was also demonstrated using this environment.

The development of the AF functionality consisted of determining appropriate control algorithms and parameters that allow the PV inverter to inject harmonic components equal in magnitude and opposite in phase with respect to existing harmonics on the feeder. As a result, cancellation of harmonic currents is obtained, leading to reduced harmonic voltage distortion in the upstream network. The principle features of the algorithm are described in Section 2.1 of the slide pack accompanying this summary, together with key issues that shaped the algorithm's development (Section 2.2).

The proposed algorithm was tested with varying harmonic levels, varying levels of irradiance, and for balanced and unbalanced harmonic currents. Additional controls were introduced to ensure that the rating of the PV inverter is not exceeded when harmonics are injected, and to avoid significant and frequent swings in the level of instructed harmonic mitigation.

Key results from the algorithm testing are shown here. Figure 1 shows feeder current with fundamental 50 Hz component (vertical axis is limited to better show harmonics) and 5th, 7th, 11th, and 13th harmonic components. The AF function is not operating.

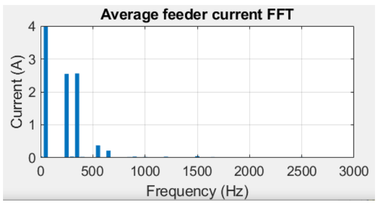

Figure 1: Feeder current harmonic components without AF operation.

In Figure 2, the AF functionality is operating, and it can be seen that the current harmonics are virtually eliminated.

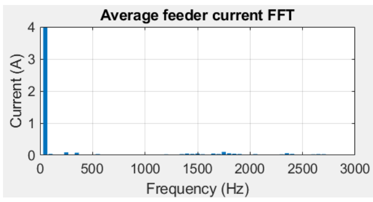

Figure 2: Feeder current harmonic components with AF operation.

This test demonstrated that with sufficient inverter capacity (i.e. the inverter not operating with full solar irradiance) the algorithm is able to alter the inverter operation and significantly reduce upstream harmonics.

Further details of the algorithm testing are contained in Section 3 of the accompanying slide pack.

Following testing and successful demonstration of the basic function of the algorithm, the impact of the proposed controller on power system performance was evaluated by using the electromagnetic transient (EMT) model developed as part of WP1. This model is a close representation of the system operating conditions for the month of October 2019.

System harmonic levels without and with AF functionality were compared. Key to assessing the impact of the algorithm was understanding the extent to which system harmonics were reduced over a three-week period that included varying levels of solar irradiance.

Figure 3 and Figure 4 show the modelled inverter current without and with AF functionality operating over a three-week period. It is clear that: (a) the inverter is much more “active” with the AF functionality operating; and (b) harmonic mitigation does not drive peak inverter current beyond levels seen without AF operation.

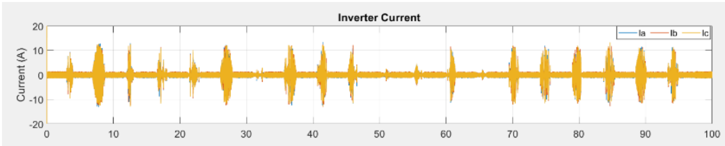

Figure 3: Inverter current, without AF functionality operating (i.e. fundamental PV power conversion only).

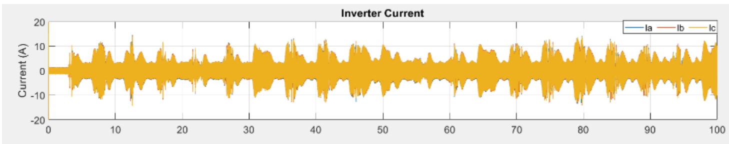

Figure 4: Inverter current with AF operation (i.e. simultaneous fundamental power conversion and harmonic injection).

Figure 5 and Figure 6 show the impact of AF operation on 5th harmonic current in the 33 kV feeder over the three week period. In Figure 5 it can be seen that the most frequent 5th harmonic current magnitude is ~1.3 A, and that currents of up to ~5.8 A occur, though the number of instances diminishes as the current magnitude increases.

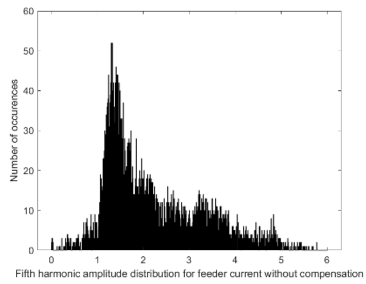

Figure 5: Frequency distribution of 5th harmonic current magnitude without AF operation.

With the AF functionality operating, a significantly different pattern of harmonic currents occurs. Only a very few instances of harmonic current above ~0.5 A occur, and the most frequent 5th harmonic current becomes ~0.1 A in magnitude.

The very few instances of higher harmonic current magnitude are associated with periods of higher solar irradiance, when the inverter does not have sufficient capacity to convert PV fundamental power and mitigate harmonics at the same time.

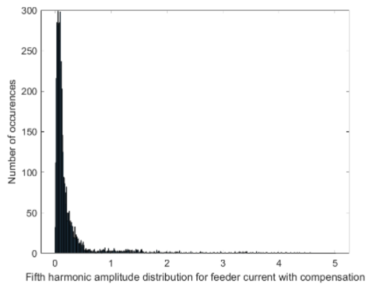

Figure 6: Frequency distribution of 5th harmonic current magnitude with AF operation.

Very similar results are achieved for the 7th, 11th and 13th harmonics, though the charts for the 11th and 13th harmonics look less dramatic due to the lower current magnitudes associated with these harmonics.

Further details of the impact of AF operation on feeder current harmonics are shown in Section 3.1 and 3.2 of the accompanying slide pack.

The demonstrated reduction in upstream feeder current harmonics has a corresponding beneficial effect on voltage harmonics at the 33 kV bulk supply point (BSP) busbar.

Figure 7 shows voltage total harmonic distortion (THD) over a three-day period. The chart highlights six THD peaks, plus three day-time variations (9 am to 4 pm).

Across the six peaks, voltage THD is reduced between 22% and 33%. During the daytime periods: a 24% reduction is achieved on Day 1; a 7% reduction is achieved on Day 2; and a 20% reduction is achieved on Day 3. Day 2 has significantly more sunshine than Days 1 or 3.

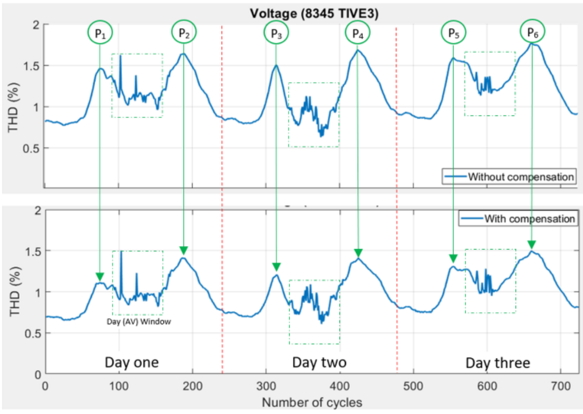

Figure 7: Voltage THD at the BSP without and with AF operation.

Considering individual voltage harmonics over the full 21 day modelled period, reductions of 14% (5th), 13% (7th), 15% (11th) and 17% (13th) are achieved. Further details of the impact of AF functionality on BSP voltage harmonics are shown in Section 3.3 of the accompanying slide pack. It should be noted that the longer term aim of the project is to consider the harmonic mitigation operation of further inverters operating on other feeders of the BSP. This is expected to further reduce voltage harmonics at the BSP busbar.

The impact of the AF functionality on an interface transformer has also been considered. Clearly the transformer losses increase with AF functionality, and under the majority of operating circumstances the losses are lower than full load losses of the transformer. On a low number of occasions, and for short periods of time, the transformer losses can be up to 15% above full load values. In practice this is very unlikely to drive hotspot temperatures to levels that would greatly accelerate insulation ageing. However, further limits on harmonic mitigation will be introduced during Work Package 3 to prevent full load losses being exceeded, and thereby take a conservative approach to the thermal impact on the transformer. Further details of the impact of AF operation on an interface transformer are considered in Section 3.4 of the accompanying slides.

Based on the discussion above and further details contained in the accompanying slide pack, conclusions from Work Package 2 are that:

- The developed algorithm takes feeder current measurements as inputs and regulates inverter switching to inject anti-phase harmonic currents to successfully achieve harmonic cancellation. The algorithm operation has been demonstrated initially through functional tests, and then by using a dynamic model of the Tiverton Network to evaluate impact of a three-week operating period.
- Factors such as phase shift of the interface transformer and delays in the acquisition of measurement data were considered. Because harmonic measurements are taken on the delta-connected side of the transformer, and harmonic injection takes place on the wye-side, an adequate phase shift has been included in the data processing stage. The final implemented design allows changing the harmonic gain not less than every 10 minutes and therefore masks the effect of delays due to data acquisition.
- The algorithm does not cause any thermal, voltage, fault level or other constraint in the network, and does not cause the power rating of the inverter to be exceeded. Thermal impact on an interface transformer has also been considered through an assessment of losses.
- The algorithm was demonstrated on an individual inverter under different operating conditions, including changing inverter output power and changing system harmonic levels. The benefits of the algorithm were shown through a detailed comparison of modelled system harmonic performance with and without the harmonic mitigation algorithm.

Detailed screenshots of the proposed algorithm have been included in the slides, and they are accompanied by a computer model.

An accompanying set of slides included here provides further detailed descriptions of the algorithm, and evidence of its performance.