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Harmonic Mitigation

Work Package Four – Hardware-in-the-Loop (HIL) testing

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Glossary

Abbreviation	Term
ADC	Analogue-to-digital
AF	Active Filter
BSP	Bulk Supply Point
FFT	Fast Fourier Transformation
HIL	Hardware-in-the-Loop
PR	Proportional resonant
PWM	Pulse-width modulation
Rms	Root mean square
SCADA	Supervisory control and data acquisition
SIL	Software-in-the-Loop
THD	Total harmonic distortion
WPD	Western Power Distribution

Executive Summary

This report presents the results from the final work package of the 'Harmonic Mitigation' project. In this work package, the algorithm developed to use the PV inverters as active filters and power source simultaneously is tested on an experimental platform. The aim of the tests is to assess that the proposed algorithm works under real-time operating conditions, i.e. under conditions that are close to the ones encountered in the real system.

The equipment used in this project consists of an OPAL-RT emulator and of a PELab power converter. The two devices are interfaced to exchange analogue and digital signals. The OPAL-RT emulator is used to execute the network model, while the PELab implements the control algorithm. This arrangement is known as 'Hardware-in-the-Loop' (HIL).

Early tests showed that the complete dynamic network model is too large to be implemented in real-time with the available equipment due to computational limitations. While it was possible to run the tests for a few seconds, corresponding to a day or two worth of real-time data, the equipment would subsequently trip due to excessive delays that led to an unstable response. Therefore, a considerable effort was placed in simplifying the network, while maintaining the essential characteristics that allowed comparing the results with the previous work packages. This effort led to the development of a simplified dynamic model. Additionally, measurement data needed to be adjusted to align the time step used in simulation with the one used in real-time. These modifications were tested with no harmonic compensation, with the aim to compare fundamental power flow and harmonic components with the ones in the original network. Voltage THD at the bulk-supply point (BSP) is the key quantity used in this project to assess the effectiveness of the proposed algorithm. In the original network model, maximum, minimum and average THD values for the entire observation period were 1.99%, 0.57% and 1.24%, respectively. The corresponding values with the simplified dynamic model were calculated as 1.95%, 0.60% and 1.25%, respectively, indicating the simplified model to be an acceptable substitution at this stage of the analysis.

The PELab was used to test the operation of the Ayshford inverter, and the aim of this work package was to duplicate the operating conditions used in WP2. To run the algorithm on the microcontroller, an additional step was added after calculation of the reference voltages, to derive the duty cycles that allow calculating the switching signals for the inverter. Tuning of the automatic gain was required as the step time in real-time is larger than in simulation. Inverter current, voltage THD at the bulk supply point and transformer losses proved to be very close to the ones obtained in WP2. More specifically, maximum, minimum and average THD values were 1.68%, 0.53% and 1.05%, respectively, in WP2, and 1.67%, 0.54% and 1.05% in HIL. These values confirm the performance already observed in simulation and the effectiveness of the developed algorithm.

This work package provided further confidence that the proposed algorithm can be used to improve power quality on the distribution network. Recommendations for future work are identified in Section 7 of this report.

1 Introduction

This report covers the work carried out in Work Package 4 of the WPD NIA Harmonic Mitigation project. The objectives of this work package include:

- Preparation of the model and the control algorithm environments for Hardware-in-the-Loop (HIL) testing.
- Validation of the Harmonic Mitigation algorithm using HIL testing.

This final work package aims at testing the performance of the proposed algorithm in a laboratory environment. The first part of the document explains the platforms used, the experimental setup and the initial tests carried out to verify the correct interconnection of the components. The second part of the document describe the test results. This report mostly focuses on HIL tests, where the inverter is physically connected to a real time digital simulator (the OPAL-RT platform) thus exchanging analogue and digital signals. However, other tests were run using software-in-the-loop (SIL) validation, where the network model and the controls are run only on the RT-LAB platform, and no physical inverter is used. SIL is used as a tool to facilitate the conversion of the network model.

The report is organised as follows:

- Section 2 provides a description of the equipment used to carry out the tests, including software and hardware, and explains how analogue and digital signals are exchanged between platforms;
- Section 3 describes the steps undertaken to prepare the network model and the development of a simplified dynamic model. Additionally, this section explains some modifications made to the PQ data to make the real-time model compatible with the Simulink model;
- Section 4 presents the results for HIL testing, including both static tests and dynamic tests. Static tests are concerned with constant loads and PV generation. Dynamic tests use the SCADA data and the PQ data as inputs to test time-varying operating conditions;
- Section 5 summarizes the lessons learned;
- Section 6 draws the conclusions for this work package and the overall project;
- Section 7 presents recommendations for future work.

Additional results from SIL analysis are presented in Appendix A.

2 Equipment description

This section documents the steps undertaken to carry out the laboratory preparation for WP4 of the Harmonic Mitigation project.

2.1 Experimental setup

Figure 1 shows the experimental setup. The two main components are an OPAL-RT emulator (OP5600) and a Taraz Technologies three-phase inverter (PELab). The OPAL-RT emulator is used to run the network model and to monitor the voltage and current waveforms, and other variables such as inverter output power and voltage THD. The PELab hosts and runs the control algorithm developed for this project, according to the input signals collected from OPAL-RT. This approach consists of 'Hardware-in-the-Loop' analysis. When performing HIL simulation, the physical system and/or plant is replaced by an equivalent computer model, running in real-time on a simulator appropriately equipped with inputs and outputs (I/Os) capable of interfacing with control systems and other equipment. In this way, the simulator can accurately reproduce the plant and its dynamics, providing comprehensive closed-loop testing without the need for testing on real systems. This approach has become a benchmark in the testing of complex controls [1]

The PELab and the OP5600 are connected via DB37 ports. These ports allow to transfer the analogue signals from the OP5600 to the PELab, and of the digital signals from the PELab to the OP5600. Figure 2 shows the back panel of OPAL-RT and the connection to PELab in details.

A laptop computer is used to run two main software packages. The first is RT-LAB, used to manage the main simulation model loaded on the OP5600, to execute the simulation and to save the variables to the workspace. The second is Keil uVision5, a software developed by ARM and used to edit the C code and program the inverter. The laptop is interfaced to the OP5600 via an Ethernet cable and to the PELab via a USB-to-USB cable. Two oscilloscopes are used to monitor the waveforms: Oscilloscope 1 is connected to the OP5600, and Oscilloscope 2 is connected to the PELab. The screen shown to the right of Figure 1 is a second monitor connected to the laptop via a HDMI port.

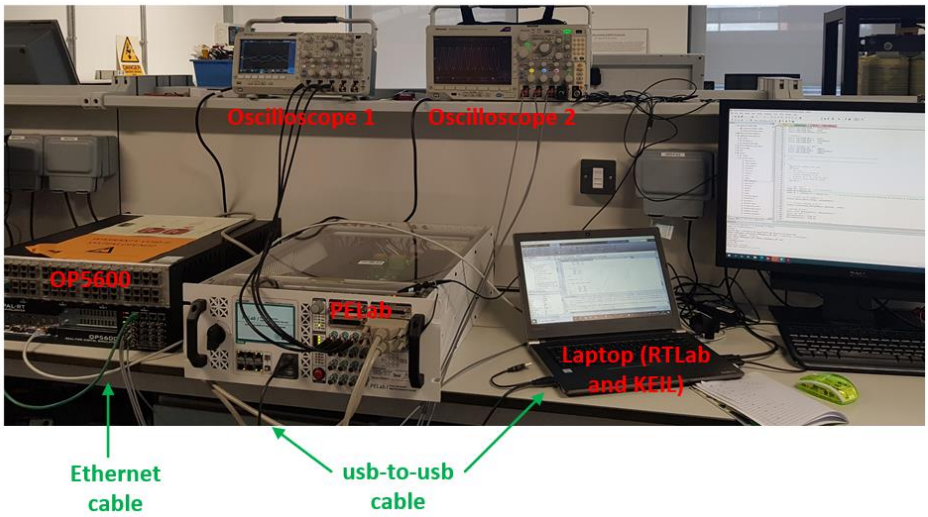


Figure 1: Set up of the experimental test bench.

Figure 2: The DB37 cables are used to connect the back ports of the OPAL-RT and the inverter.

2.2 OPAL-RT and RT-LAB

RT-LAB is fully integrated with MATLAB/Simulink (the software that was used to develop the control system) and allows Simulink models to be imported and edited in RT-LAB. Although the model developed in the previous work packages can be used, some modifications are required for the model to run on the OP5600 platform. The first set of modifications include a restructuring of the model components: while in simulation the model and the monitoring blocks run on a single device (i.e. the laptop), for the experimental analysis the model is split in two main subsystems. These two subsystems are compulsory in RT-LAB: the first subsystem, 'SM_computation' runs on the emulator (OP5600) and the second, 'SM_gui', runs on the laptop, respectively. The two subsystems and their allocation are shown in Figure 3. The 'SM_computation' subsystem solves the network model at each time step and records the variables (voltage, current and power). The 'SC_gui' is the 'graphical

user interface' that allows displaying the results for checking the performance of the model on the laptop while the model is running. When the simulation is stopped, the results are sent to the computer memory.

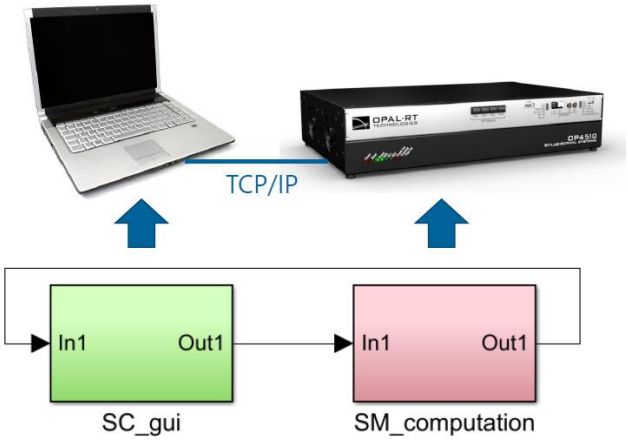


Figure 3: Overview of the model configuration for real-time execution (stock image from OPAL-RT).

Additionally, some specialist blocks are required: these blocks are responsible for handling the communication between the laptop and the OPAL-RT emulator and to manage the OP5600 memory.

The model needs to be simplified to achieve real-time-simulation. The simplification of the model aims at reducing the processing time. This was carried out by removing monitoring blocks irrelevant for this Work Package and reducing data sent to the scopes. Although the model has been simplified, it has been carried out so that the integrity of the model is maintained, to allow comparison with the results in the previous work packages. Finally, the sampling time in OPAL-RT needs to be increased compared to simulation to run the model in real-time. Figure 4 shows an example of interface window used to monitor the number of overruns: for the example shown in this figure, the sampling time is 50 µs.

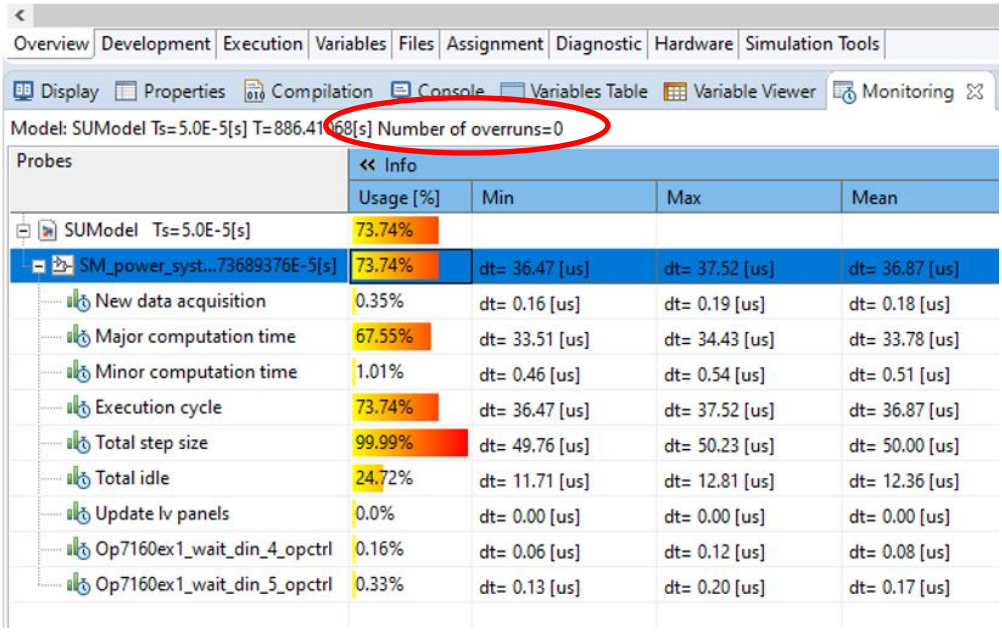


Figure 4: RT-LAB interface used to communicate with the inverter.

2.2.1 Example of integration issues: data loss

Some data loss in the scope of the graphical user interface (GUI) were observed when testing started, as shown in Figure 5. The data loss is due to the computational limitations of the laptop connected to the OPAL-RT platform. This effect was mitigated by applying two solutions: 1) the 'Probe control' settings on the RT-Lab platform were modified to reduce the number of samples per signal; 2) a 'rate transition block' was introduced in the model to reduce the number of datapoints sent to the workspace. These modifications improved the results, as shown in Figure 6, where data loss is visibly reduced.

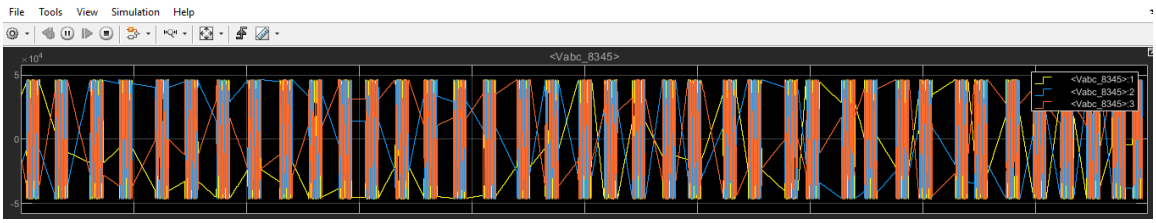


Figure 5: Voltage waveform at TIVE3: initial results with significant data loss.

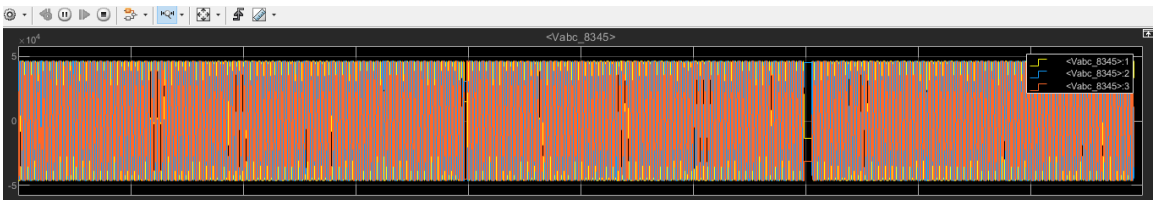


Figure 6: Voltage waveform at TIVE3: updated results where data loss is significantly reduced.

It is worth emphasizing that the data loss is only affecting the graphical display: the analogue outputs and the data exported to the MATLAB workspace from the OPAL-RT simulator do not experience any data loss. This can be easily verified by observing that the oscilloscope connected to OPAL-RT shows a continuous and smooth waveform, as shown in Figure 7 which shows the voltage at TIVE3.

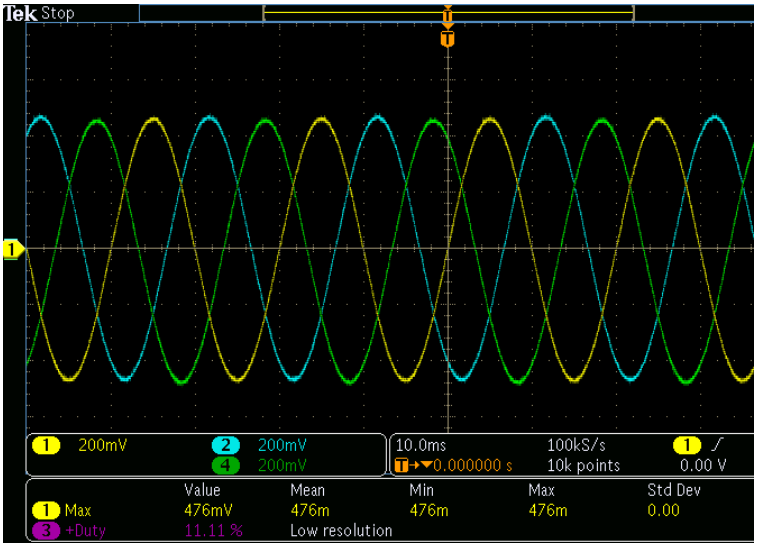


Figure 7: Screenshot from Oscilloscope 1, illustrating a sample analogue output.

2.3 PELab and Keil software

The second part of the preparation consisted of programming the PELab. PELab programming is carried out using the Keil uVision5 software – this software allows writing a C-code that is then compiled and sent to the PELab microcontroller. The Keil uVision5 software runs on the laptop shown in Figure 1. Once compiled, the code is sent to the PELab via a USB-to-USB cable.

The PELab includes an industrial grade controller module that is specially designed for power electronics applications. The controller uses the ST Microelectronics ARM® Cortex® M7 and M4 dual core STM32H745BI microcontroller. For this project, a single core is used, specifically the M7 microcontroller. The code structure includes a low-level programming algorithm (provided by the manufacturer), drivers, and the high-level code converted from Simulink using the code generating features in MATLAB/Simulink. The inputs to the PELab are analogue signals from OPAL-RT and the digital outputs are the switching signals to command the inverter.

2.3.1 Analogue inputs

The analogue inputs are the signals sent from OPAL-RT to the inverter. These signals must be limited between +10 V and -10 V: outside these boundaries, the embedded inverter

protection will activate. Therefore, current and voltage readings fed to the PELab are a scaled replica of the readings from OPAL-RT. Because the analogue-to-digital converter (ADC) is using a 16-bit resolution, -10 V corresponds to 0, 0 V corresponds to 32768 ($2^{16}/2$) and +10 V corresponds to 65535 (2^{16}). To reconstruct the original value, a scaling factor needs to be applied first to the analogue readings: 10/32768. Then, the value needs to be scaled by 32768 to obtain negative numbers. The code used to implement voltage and current scaling is shown in Figure 8. It is important however to observe that the signals used in this project are up to 1 V, that corresponds to 1 p.u., because the controller has been developed using per unit quantities.

```
/* set the offsets and multipliers according to the connections */
for (int i = 0; i < 16; i++)
{
  adcOffsets[i] = 32768;
  adcMults[i] = 0;
}

mults.Ih1 = 10.0f / 32768;
mults.Ih2 = 10.0f / 32768;
mults.Ih3 = 10.0f / 32768;

mults.Ia = 10.0f / 32768;
mults.Ib = 10.0f / 32768;
mults.Ic = 10.0f / 32768;

mults.V1 = 10.0f / 32768;
mults.V2 = 10.0f / 32768;
mults.V3 = 10.0f/ 32768;
```

```
/* convert the values */
int i = 15;
do
{
  fResults[i] = (ul6Results[i] - adcOffsets[i]) * adcMults[i];
} while(i-- != 0);
```

Figure 8: Scaling of analogue input in the C code and conversion of digital signals to analogue values.

2.3.2 Digital outputs

The digital output of the PELab are the switching signals. In the modelling environment (i.e. the model used in WP2 and WP3 a pulse-width modulating (PWM) block was used to generate the switching pulses for the inverter, based on the voltage reference signals.

In the experimental setup, the microcontroller requires an intermediate step, i.e. the calculation of the duty cycles from the reference voltage. The switching pulses are then calculated from the duty cycles by low-level code programmed in the microcontroller (the concept of 'duty cycle' is described in the literature review report for WP1) and they are sent to the inverter model included in OPAL-RT. In this way, the controller is included 'in the loop' and it is interfaced with the plant – in this case, the network.

Figure 9 shows a part of the C code used to calculate the duty cycles: in the first three rows, the reference voltages (sPWMabc) are scaled, and a counter is used to calculate the

pulses for each switching cycle (i.e. 50 µs for 20 kHz switching frequency). The duty cycle is calculate per each phase – referred as duties[0], duties[1] and duties[2] in the code.

The resulting digital outputs (i.e. the switching signals) are shown in Figure 10. The code used in this work package results in the generation of six digital outputs: the first two signals are for phase a, then phase b and phase c follow in pairs. For each phase, the second signals is the logical negation of the first, as only one switch per phase can be in the 'on state' (i.e. the switching signal is equal to unity).

```
fReturnPWM[0][iCounterPWM] = sPWMabc.fC / divduty;
fReturnPWM[1][iCounterPWM] = sPWMabc.fA / divduty;
fReturnPWM[2][iCounterPWM] = sPWMabc.fB / divduty;

static int iAppPWM;

if(iCounterPWM+ iShift > 499)
  iAppPWM = iCounterPWM + iShift - 499;
else if(iCounterPWM+ iShift < 0)
  iAppPWM = 499 + (iCounterPWM+ iShift);
else
  iAppPWM = iCounterPWM+ iShift;

duties[0] = fReturnPWM[0][iAppPWM];
duties[1] = fReturnPWM[1][iAppPWM];
duties[2] = fReturnPWM[2][iAppPWM];

duties[0] = (duties[0] * 0.5f) + 0.5f;
duties[1] = (duties[1] * 0.5f) + 0.5f;
duties[2] = (duties[2] * 0.5f) + 0.5f;
```

Figure 9: Calculation of duty cycle for phase a, b and c (0, 1 and 2, respectively) in the C code.

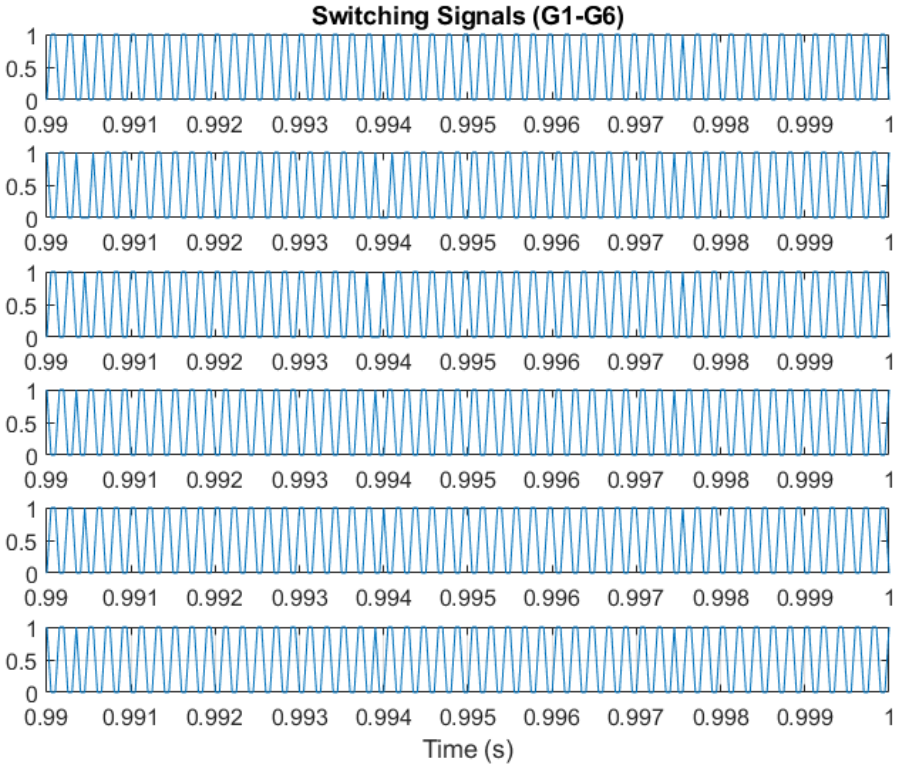


Figure 10: Example of switching signals, used as digital input to OPAL-RT.

The inverter model used in WP2 and WP3 required 12 digital signals, i.e. four per phase: this model was chosen as it was the only one available for the purpose of representing a three-phase inverter in Simulink. OPAL-RT includes more inverter models, so at the end two choices were possible for the experimental validation:

1) to use a six-pulse inverter model, using the six digital inputs from PELab
2) to use a twelve-pulse inverter model and calculate additional digital inputs.

Some discussions took place with Mathworks and OPAL-RT technical support to identify the best approach. As part of this investigation, the use of a six-pulse inverter available in OPAL-RT was investigated, and numerous tests were run with various inverter configurations and switching signals. It is important to note that for the purpose of this work the use of a six- or twelve-pulses configuration does not have any impact. The twelve-pulses model provides more flexibility as it allows representing inverters where the dc-link is made of two capacitors with the common point grounded – effectively, it provides an extra node. However, in the case of this project the dc-link is interfaced with the PV panel, and therefore the ground connection is not used and the additional switching pulses per phase are obtained as a duplication of the six pulses provided by PELab [2].

However, these tests didn't lead to satisfactory results, as the current waveform presented excessive distortion. Therefore, the team reverted to the use of a twelve-pulse inverter, where the switching signals are obtained by duplicating the six pulses shown in Figure 9. Adopting the twelve-pulse inverter resulted in reduction of the switching noise and cleaner

waveforms. The generation of the twelve pulses from the six analogue signals is shown in Figure 11.

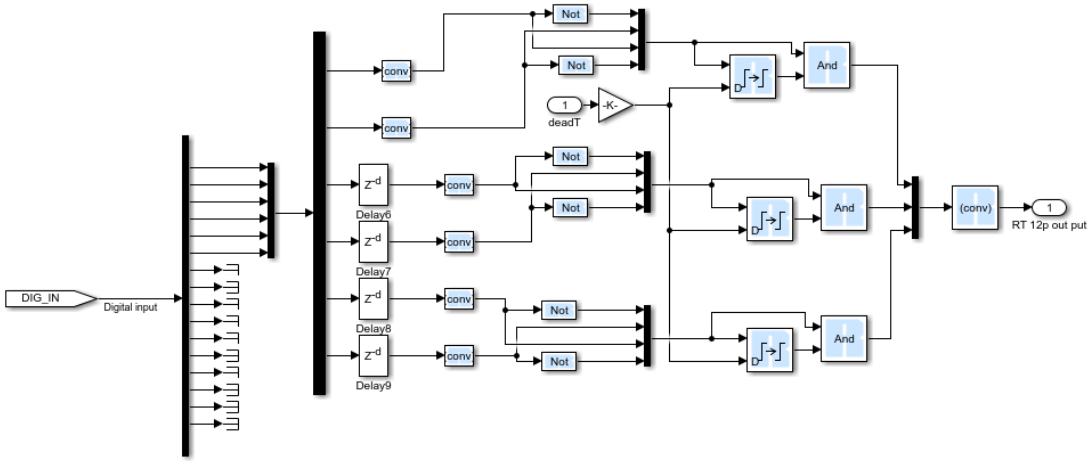


Figure 11: Duplication of the digital signals from the inverter to generate 12 switching pulses.

2.4 Visualising the results in the oscilloscopes and in RT-LAB

Two oscilloscopes are connected to the equipment, as shown in Figure 1. The first oscilloscope is connected to OPAL-RT and the second is connected to PELab. The number of channels available for each oscilloscope is four, and typically three channels are used to display three-phase quantities.

The first oscilloscope is used to monitor the grid signals from OPAL-RT. This oscilloscope is connected to the front panel. It is important to observe that the output signals from OPAL-RT are in p.u., and additionally a 0.1 scaling is applied to the front panel (this is an internal calculation that cannot be altered). Therefore, typically the amplitude of the voltage signal is in the order of 100 mV peak. In this work package, this oscilloscope is used to monitor TIVE3 voltage.

The second oscilloscope is used to monitor the input of the PELab – i.e. the inverter voltage or the inverter current. In this case, the quantities are in p.u. It is worth noticing that the fast digital output cannot be monitored with the oscilloscope (as they are not available in the interface). However, these signals can be saved and plotted directly in the workspace.

In this report, the results presented are mostly generated from the workspace as this approach allows to provide figures that are more readable – i.e. they include axes and labels, and they can be easily zoomed into the region of interest. Additionally, this approach allows overlapping the results with the ones obtained in WP2. However, in some cases oscilloscope screenshots are provided to show the output from the equipment. Additional oscilloscope results are included in Appendix C for illustrative purposes.

2.5 Examples of waveforms from initial setup

This section presents some waveforms obtained from the initial setup of the equipment and intended to validate the basic model functionalities and interconnections, as well as the scaling. These waveforms do not represent part of the formal testing.

2.5.1 Fundamental current results

Numerous tests were run to tune the inverter control algorithm. The figures below illustrate some results in terms of voltage and current waveform.

Figure 12 shows the voltage at TIVE3 (the BSP): this is a clean waveform at 50 Hz since there are no harmonic loads in the model, and the inverter under consideration is connected at a different busbar. Figure 13 and Figure 14 shows the voltage at Ayshford 33 kV as recorded in OPAL-RT and from Oscilloscope 1, respectively.

Figure 13 and Figure 14 are not identical as the oscilloscope clock is not linked to the simulation time – therefore, it is not possible to identify the section of the workspace matching the oscilloscope screenshot. Additionally, the scaling in the two graphs is not the same: while the data from the workspace can be scaled to show the actual voltage amplitude (Figure 12 and Figure 13), the oscilloscope shows results in per units. More specifically, one division in the oscilloscope corresponds to 50 mV and the peak voltage is 100 mV (Figure 14). Therefore, 100 mV corresponds to approximately 46.67 kV (33 kV x √2).

In both waveforms, a small distortion can be observed. As explained above, these waveforms are only representing initial results, and more tunings and checks will be carried out in the next sections.

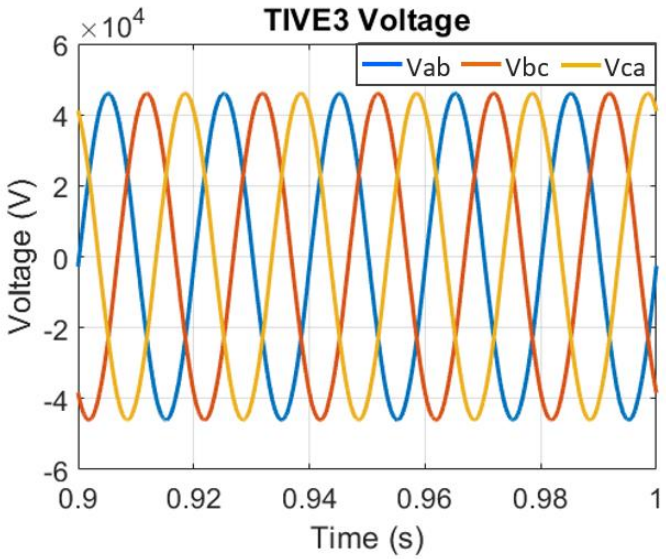


Figure 12: Voltage at TIVE3 (workspace).

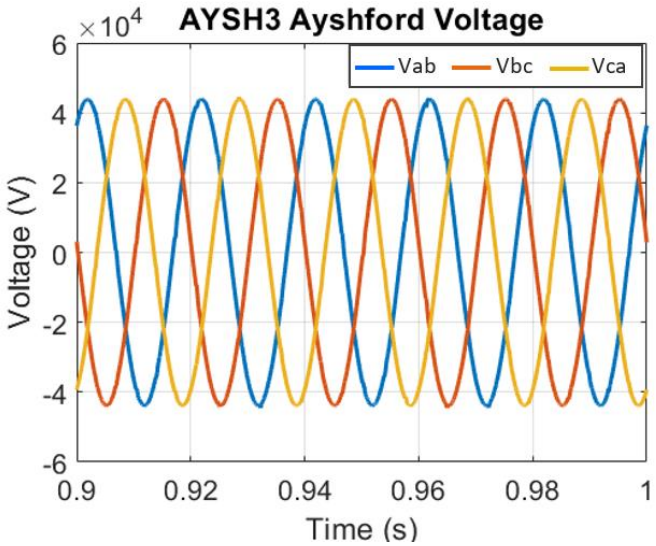


Figure 13: Voltage at Ayshford 33 kV (Workspace).

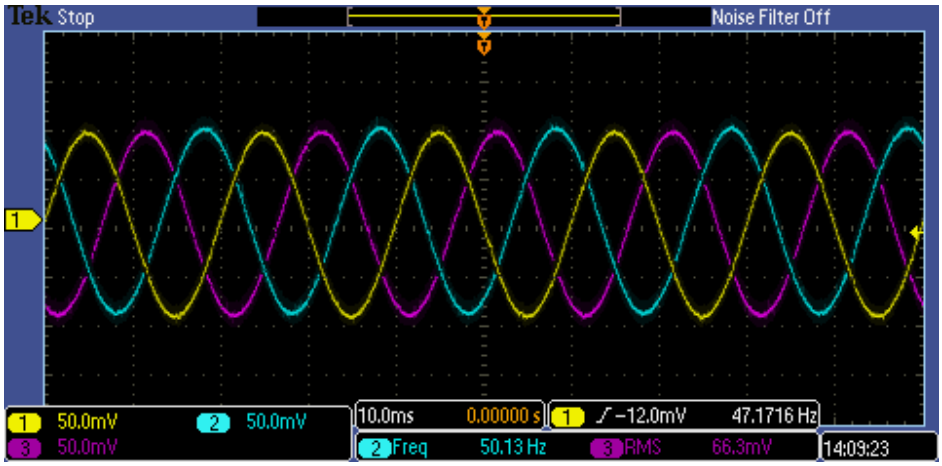


Figure 14: Voltage at Ayshford 33 kV (Oscilloscope 1).

Figure 15 and Figure 16 show the inverter current at Ayshford 33 kV, using the workspace data and Oscilloscope 2 respectively. In this case, the effect of the switching noise is slightly more visible, but still acceptable.

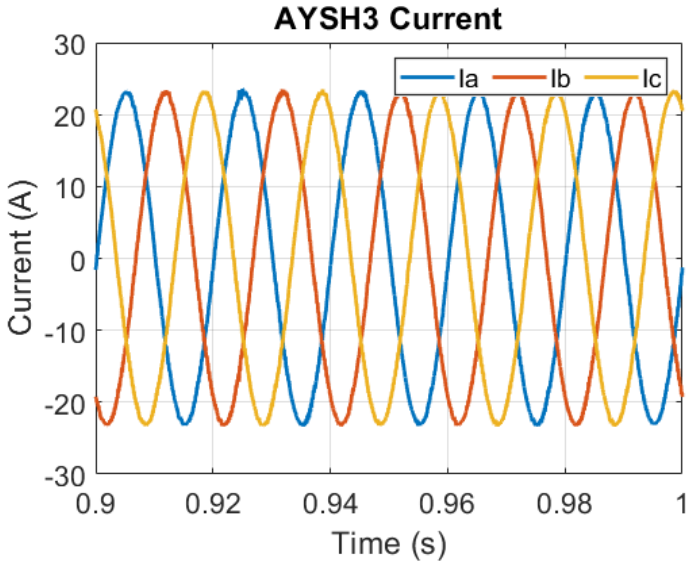


Figure 15: Inverter current at Ayshford 33 kV (workspace).

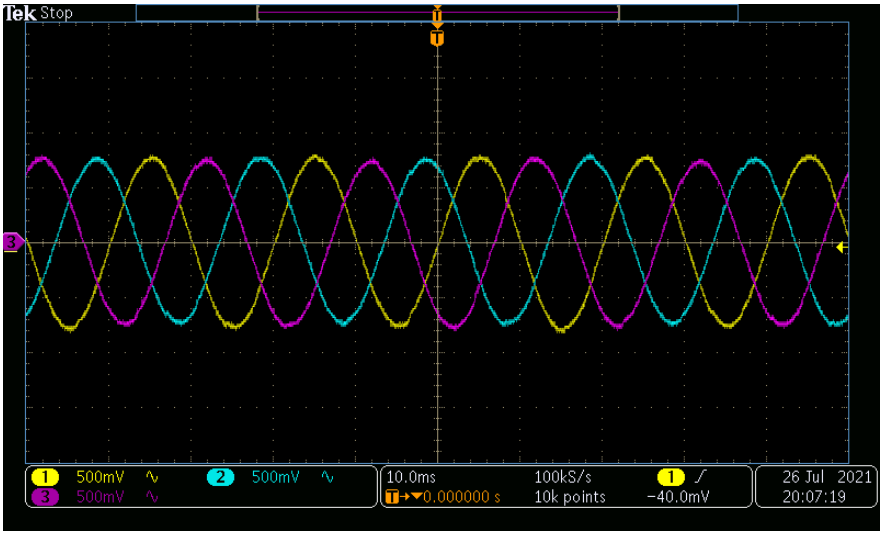


Figure 16: Inverter current at Ayshford 33 kV.

2.5.2 Harmonic validation

The inverter current with all harmonics of interest for the project included is shown in Figure 17, while the corresponding spectrum is shown in Figure 18. Both figures indicate that the desired harmonics are injected by the inverter along with other harmonics (mainly due to switching action) that are relatively small and hence negligible in amplitude. The fundamental current is much larger than the harmonics, and the graph is a zoomed version in order to show the harmonics more clearly. Labels have been added to indicate the amplitude of each harmonic of interest.

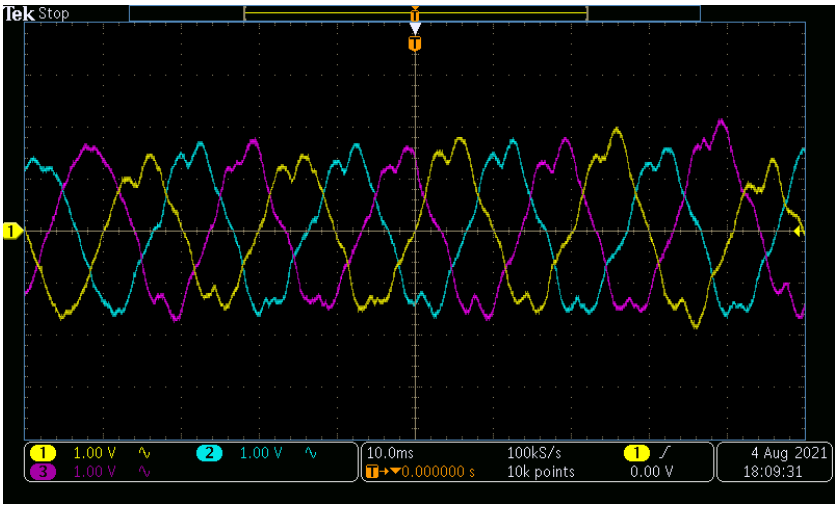


Figure 17: Inverter current from the oscilloscope when all harmonics are included.

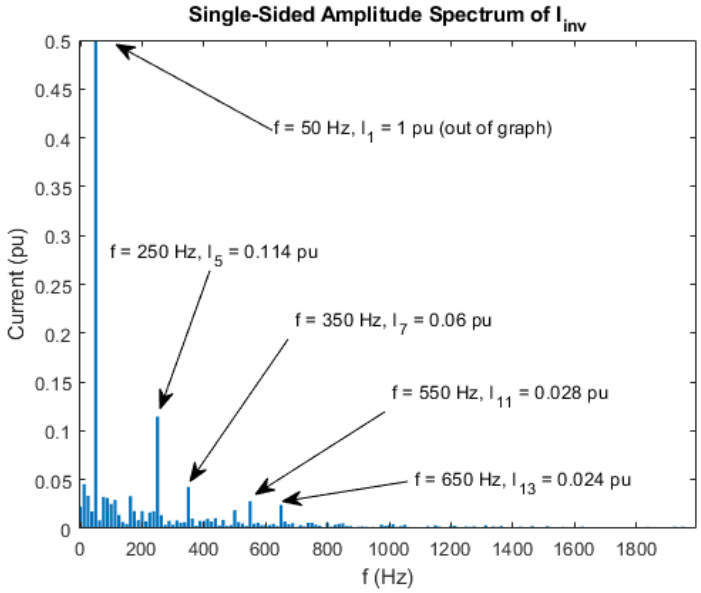


Figure 18: Harmonic current FFT.

2.6 Conclusions

This section described the equipment to be used to carry out the experimental work in WP4: the two main components are the OPAL-RT platform, used to run the network model, and PELab, used to run the control algorithm. The equipment is interfaced by using DB37 cables to exchange analogue and digital signals. A laptop is then used to program the equipment, manage the tests and process the results. Two oscilloscopes are also used to monitor the experiments.

Some results have been shown to demonstrate the correct operation of the equipment, while more detailed description of the models and the tests will be presented in the next sections.

3 Network model preparation

An overview of the system under consideration is shown in Figure 19, while more details are provided in Appendix A, and in the previous reports, available on the project website [3].

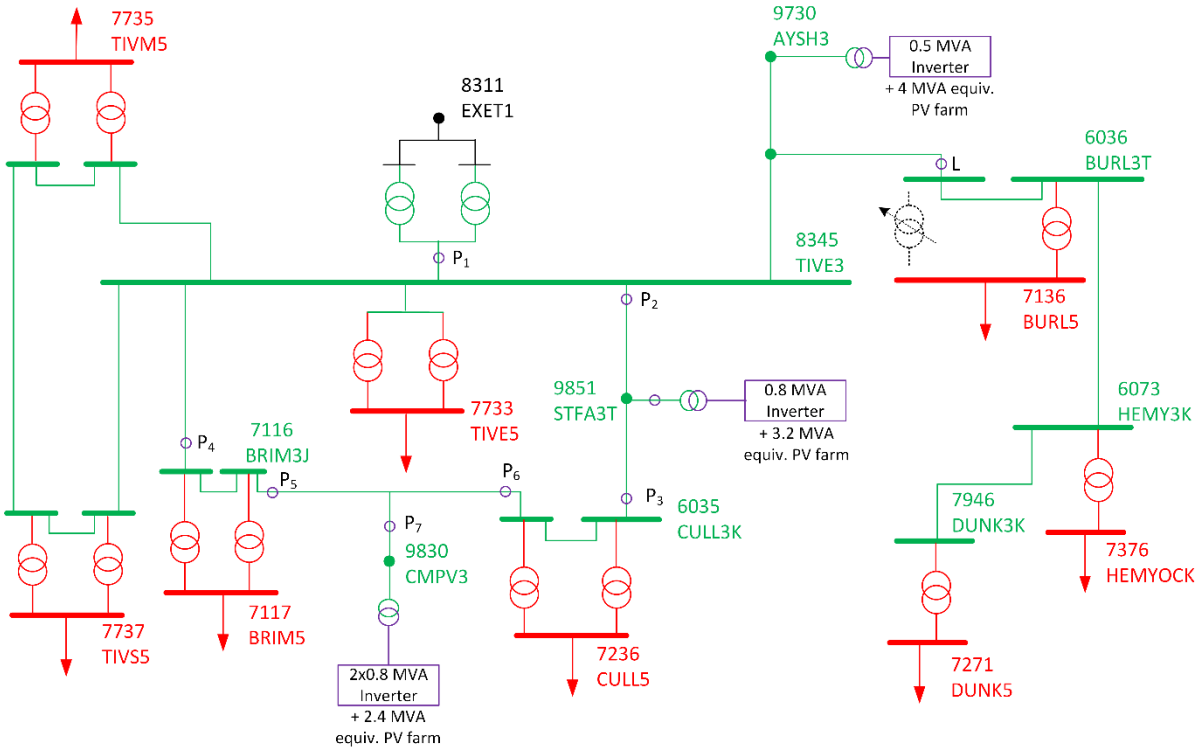


Figure 19: Overview of the Tiverton network, including the PV farms and the measurement points (P_1-P_7 and L).

3.1 Static model

Using a simplified approach and process described in Section 2.2, Simulink model was imported into RT-LAB and a static model of the network was developed. Besides the considerable time saving in using the imported model, an additional advantage consisted in the use of identical blocks, thus allowing for consistency between the models used in different work packages and with different platforms. For the static model, the loads were considered as constant – i.e. with a fixed active and reactive power demand. Similarly, to the steps taken in WP2, this allowed verifying the correct behaviour of the network model and of the PELab.

3.2 Dynamic model

In order to replicate the results obtained in WP2, it was necessary to run the model for the entire observation period. Therefore, the measurement datasets were imported into the network and used to develop a dynamic model. The measurement datasets consisted of power quality (PQ) data with 10 s resolution and SCADA data with 30 min resolution.

In order to import these data in RT-Lab, two different OpFromFile blocks are required, as the two data sources have a different resolution. These blocks are shown in Figure 20 The first block is used to read the PQ data (File: PVnew.mat), the second block is used to read the SCADA data (File: Oct_scada1.mat).

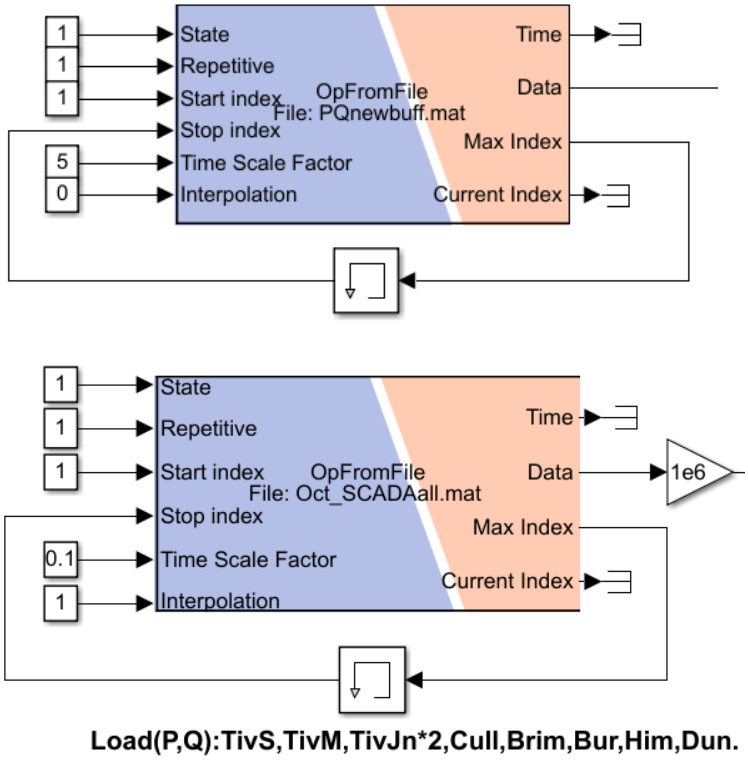


Figure 20: OpFromFile blocks.

Some adjustments were required to the model settings in order to run the dynamic model in real-time, using the imported data.

The adjustment was related to the time step: while it was possible to achieve an 8 µs time step in Simulink, and 50 µs with the static model in RT-Lab, the time step needed to be increased to 100 µs to accommodate the large network and the large data set used in the static model. This limitation is mostly related to the speed of the processor used in OPAL-RT.

The second adjustment was related to some setting in the OPFromFile block used for the SCADA data. This dataset has a resolution of 30 minutes, corresponding to 0.1 seconds in simulation. When the data was imported in the RT-LAB model, it resulted in step change of the load demand, thus resulting in significantly different results from the simulation, and unrealistic behaviour. This issue was rectified by activating interpolation in the OpFromFile to ensure a gradual change and obtaining a behaviour similar to the one shown in WP2 and WP3.

The last adjustment was related to the time resolution of the PQ data, that was recorded with a high resolution at 10 s intervals. To facilitate the description of this aspect, the mapping of the dataset in different domains (measurement, simulation and SIL/HIL) is visualised in Figure 21.To maintain consistency with the SCADA dataset, the PQ data was using a resolution of 0.556 ms in simulation (WP2 and WP3). However, this time interval cannot be used in RT-LAB because the time stamp associated with the data must be an integer multiple of the simulation time step. The closest acceptable resolution was 0.5 ms, however, using this value led to a shift in the results obtained in RT-LAB compared with the ones obtained in Simulink (WP2). This behaviour can be understood by referring to Figure 22, where the discrepancy between the run times in different domains are shown for one day, and for the entire simulation time.

Without the introduction of the explained adjustments, errors such as the ones shown in Figure 23 and Figure 24 would be observed in the output. In these figures, the discrepancy between RT-LAB and the simulation results (WP2) is evident both at fundamental component and at harmonic components.

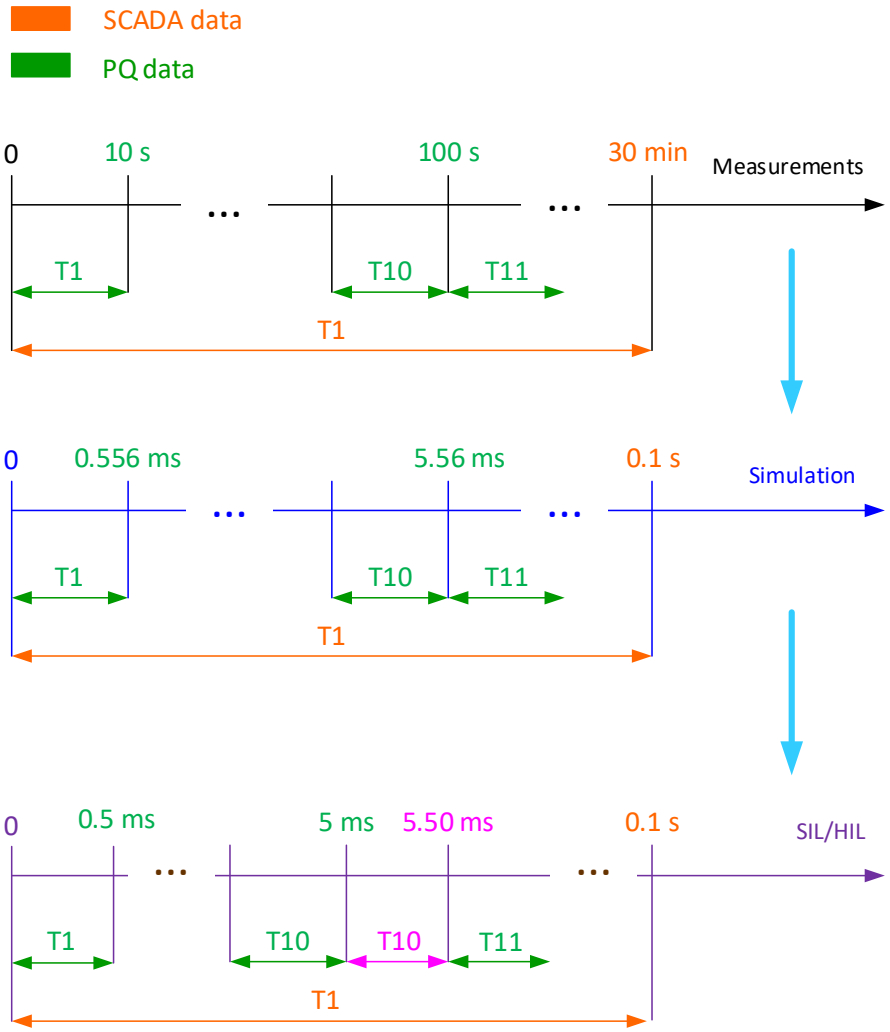


Figure 21: Mapping of SCADA data and PQ data in different domains.

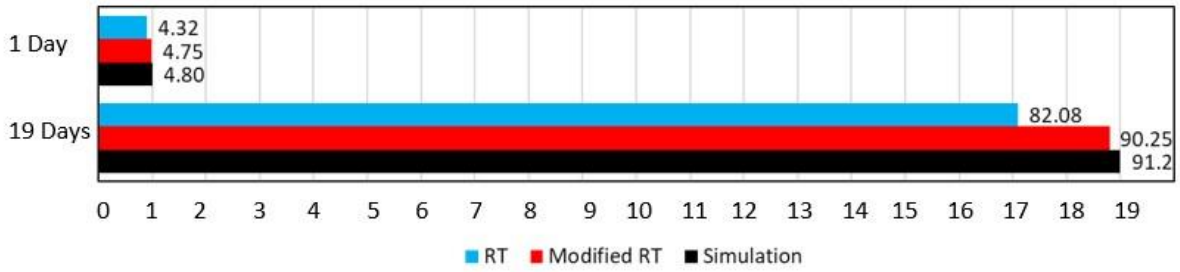


Figure 22: Comparison of the simulation times for RT (original, with no adjustment of the data), Modified RT and Simulation. The modified RT and the Simulation times match very closely.

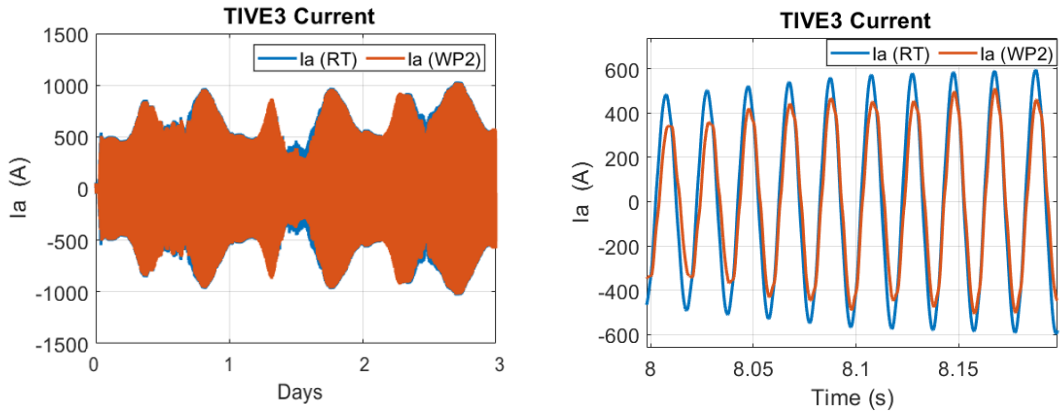


Figure 23: Fundamental current at TIVE3 showing a significant error due to time shift. Original and zoomed in version.

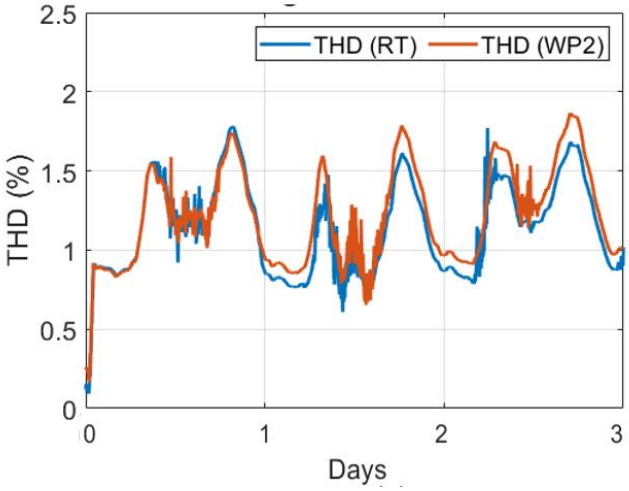


Figure 24: Voltage THD at TIVE3 – significant error due to time shift.

To overcome this problem, the team decided to duplicate one point every ten for the PQ data to better align the results (therefore, compensating for the compression of the time scale from 0.556 ms to 0.5 ms). This decision was made by observing that the PQ data had a very high resolution, and they provide a sample of a typical operating condition. Therefore, duplicating one every ten points does not deviate too much from the realistic operation, but allows comparing the results with the previous work packages. This process is schematically shown in Figure 21, where the duplicated point is shown using magenta colour. Figure 22 shows the comparison of 1 day and the entire observation period between original RT, modified RT and simulation. The modified RT and simulation were very close.

After applying the correction described above, the match between real-time and simulation was significantly improved, as shown in Figure 25-Figure 27

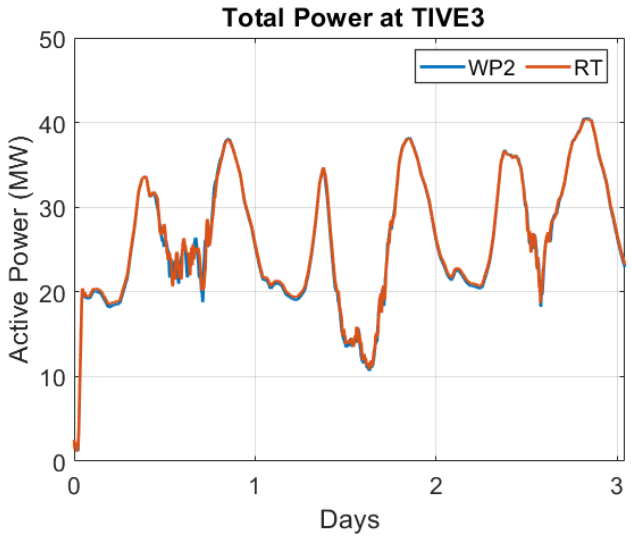


Figure 25: Total power at TIVE3 for three days after correction of the PQ data.

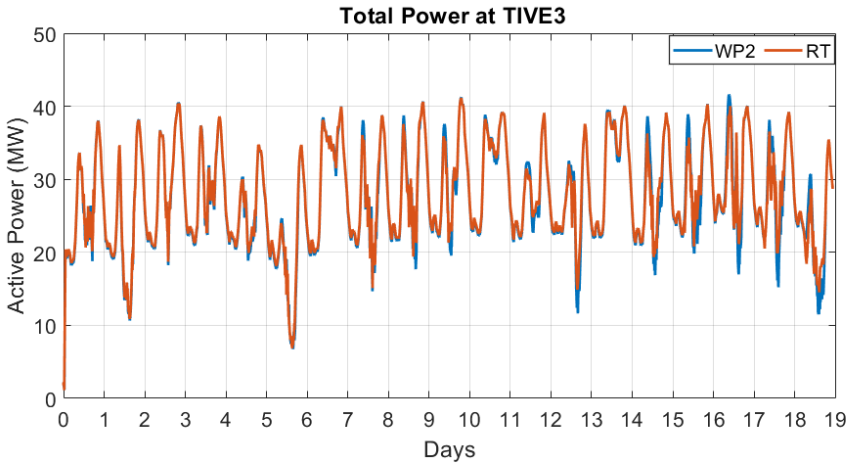


Figure 26: Total power at TIVE3 for entire observation period after correction of the PQ data.

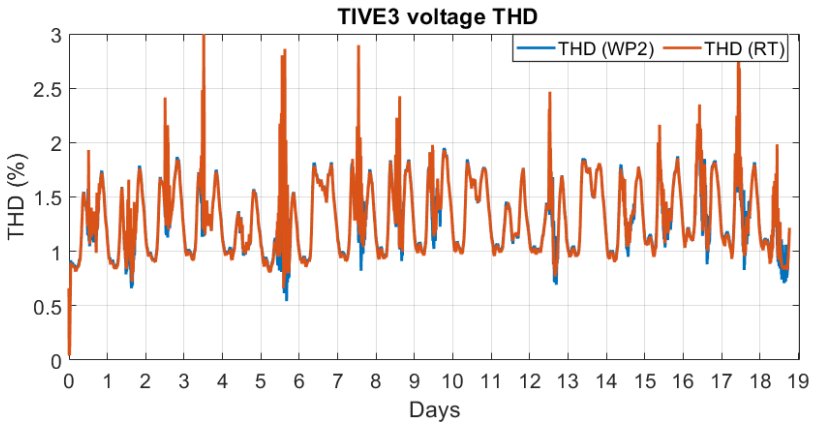


Figure 27: Voltage THD at TIVE3 for the entire observation period after correction of the PQ data.

A detailed comparison in terms of harmonic components for two testing conditions is shown in Figure 28.

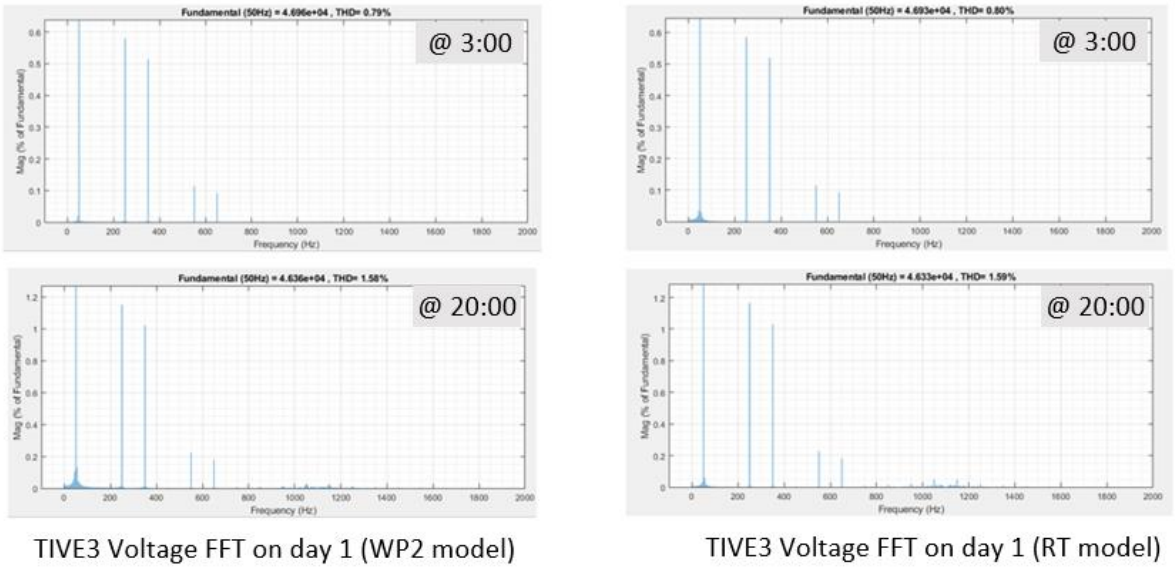


Figure 28: Voltage FFT at two points in Figure 27, comparison of WP2 and RT results for two hours in Day 1.

During HIL tests, it was observed that the time scale needed further tuning to improve the results toward the end of the observation period. Additional adjustments to the time scale were carried out and they will be described in Section 4.2.

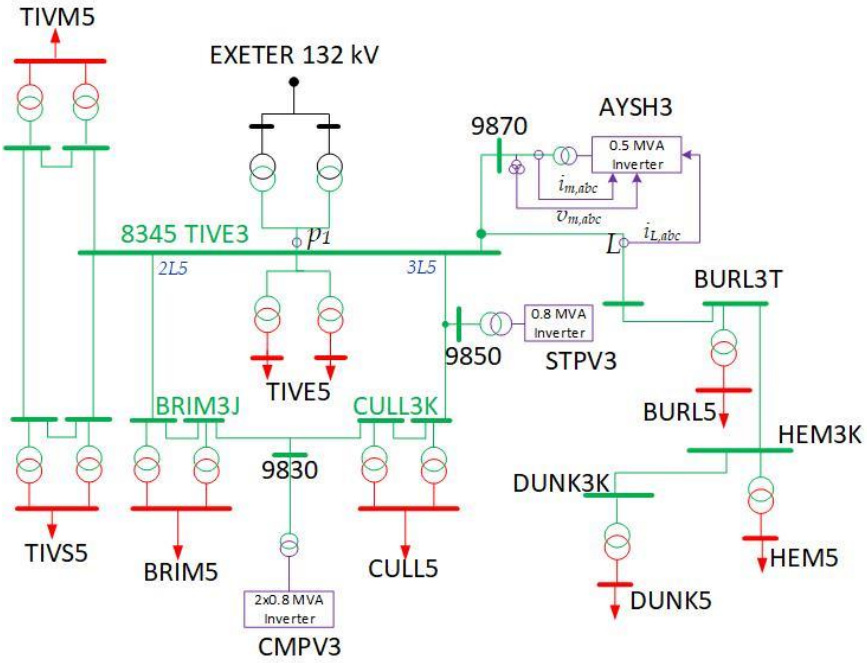
3.3 Simplified dynamic model

Introduction of the dynamic model to HIL testing led to inverter instability after running for a few cycles and eventually tripping. This issue was investigated thoroughly and mitigated. Initially, work was done on the inverter code to improve the switching pulses generation, and consequently the inverter was able to run for a few seconds (as it will be described in Section 4). However, this didn't allow running the tests for the entire observation period. Therefore, the attention was posed on the grid simulator (OPAL-RT).

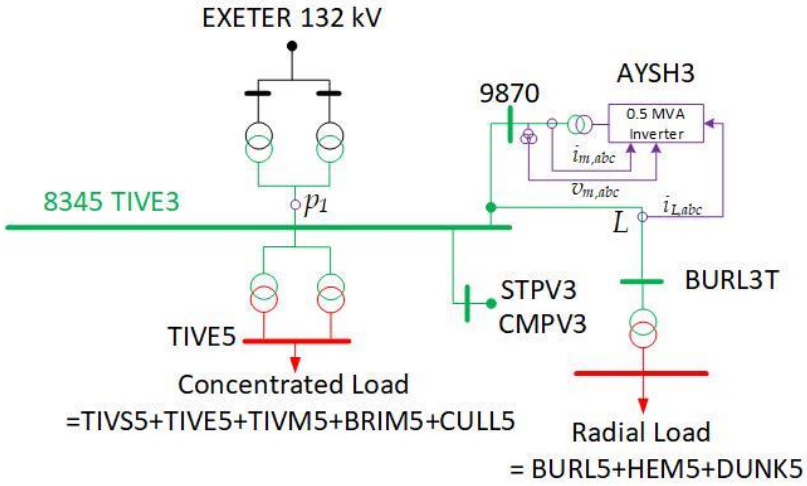
It was concluded that the instability observed is caused by the computational effort required to run the network in real time, and accumulation of delays in the transmission of analogue and digital signals between OPAL-RT and the inverter. Therefore, it was decided to further simplify the model used in OPAL-RT, and generate a simplified dynamic model, that still allowed to test the proposed functionality, using a smaller network.

The simplified model includes a single load connected at TIVE3 busbars, obtained by combining all SCADA data, and as a result, the rating of the transformer connected at TIVE3 is increased to 50 MVA. The PV farms at Cullompton and at Stoneshill are represented by means of equivalent models. The single-line diagrams of the original network model and the simplified network are shown in Figure 29.

This simplification of the network model required further verification to check if the results of the previous work packages could still be matched. In the remaining of this section, validation of the model without compensation will be carried out, while in Section 4, validation of the algorithm with HIL will be presented.



a)



b)

Figure 29: Comparison between a) the complete network model and b) the simplified network model network for HIL analysis.

3.4 Simplified dynamic model validation

The first check was carried out on power measured at TIVE3. It was observed that due to the lack of transmission lines and transformer (and hence lack of losses), the use of the lumped model resulted in higher power measurement at TIVE3, compared to full model. After some tuning, it was concluded that the lumped load power needed to be reduced by 8%. This led to a close match with the results of WP2, as shown in Figure 30.

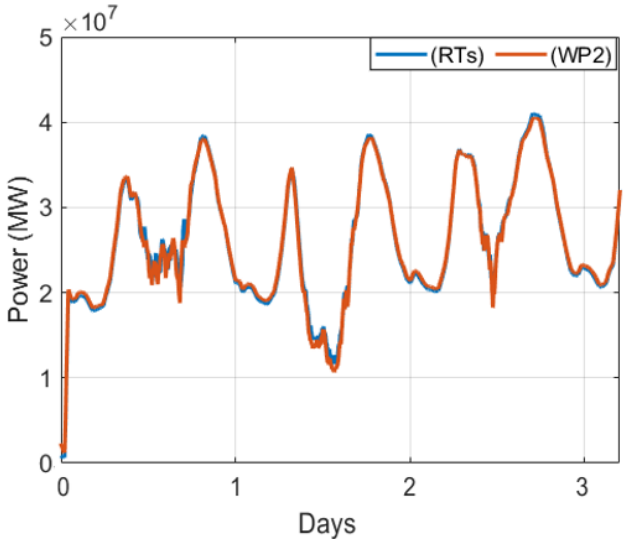


Figure 30: Power comparison at TIVE3 between WP2 and the simplified OPAL-RT model.

The second verification parameter was voltage THD at TIVE3. As indicated in Figure 31, the results are very close to the ones obtained in WP2, however, some discrepancies can be observed toward the end of the observation period. This is due to the fact that the adjustment in the PQ data described in Section 3.2 still does not result in a perfect match of the time scale between simulation and real-time.

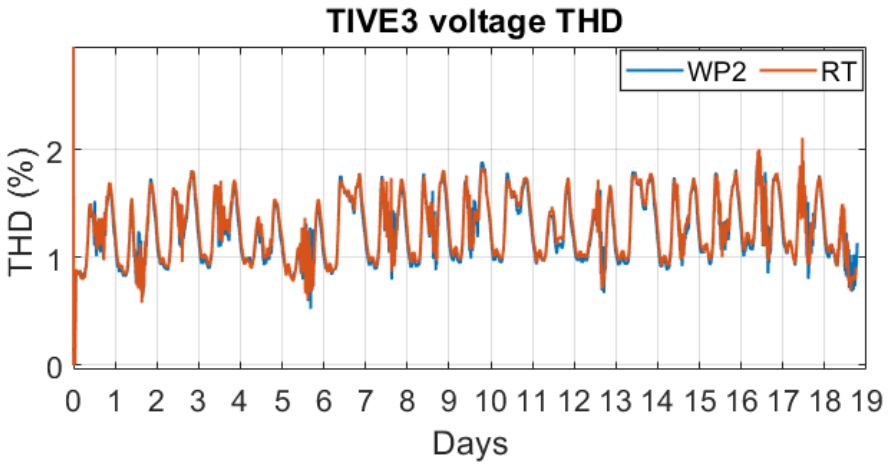


Figure 31: Voltage THD comparison between WP2 results and real-time with concentrated load without compensation.

In order to further improve this behaviour, it was decided to add some 'zero' values to the PQ data at the end of day 5, day 10 and day 15. These times corresponds to the night period, where the generation from the PV farms is absent, and therefore the proposed change has a correct physical interpretation. As a result, the match with WP2 results is

significantly improved, as shown in Figure 32. Detailed comparison of THD results for the entire period is shown in Table 1.

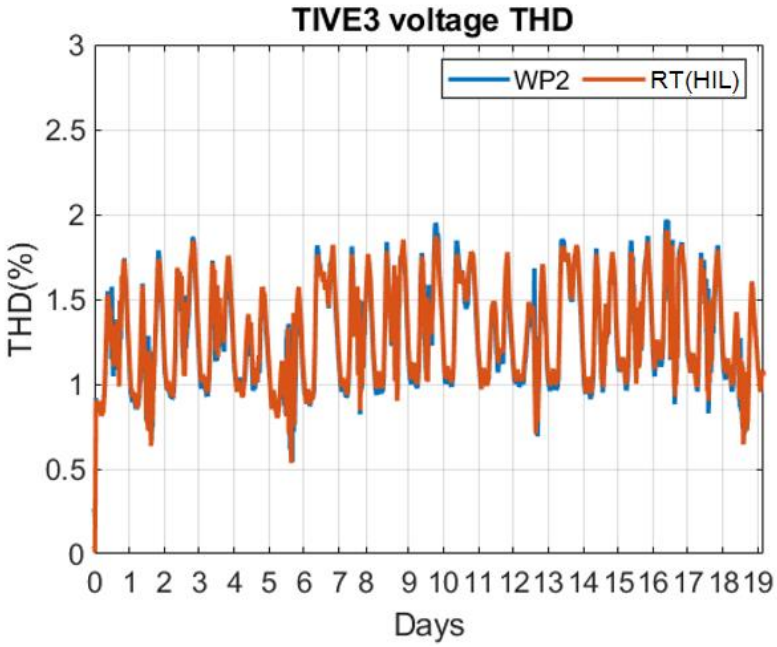


Figure 32: Final THD results in HIL (without compensation).

Table 1: Comparison of THD for WP2 and RT (without compensation).

	WP2 (THD) for entire period (%)	RT (THD) for entire period (%)
Mean	1.24	1.25
Max	1.99 @ t= 78.9 s (16 d, 9:30 h)	1.95 @ t= 78.9 s (16 d, 9:30 h)
Min	0.57 @ t= 26.90s (5 d, 14:40 h)	0.60 @ t= 26.90 s (5 d, 14:40 h)

Based on the results presented above for both fundamental frequency and harmonics, it can be concluded that the simplified network model is able to duplicate the network conditions studied in the previous work package. Therefore, this model can be used to carry out HIL analysis and validation of the proposed algorithm, as it will be shown in Section 4.

3.5 Conclusions

This section presented the steps undertaken to prepare the network model run on the emulator. Initially, a static model was used, and then a dynamic model was developed by importing the measurement data set. It was observed that adjustments to the time scale of

the PQ data were required to match the simulation results, as the time step used in real-time is larger than the one used in simulation.

After running some tests with the inverter, it was concluded that it was necessary to reduce the network model in order to be able to run the tests for the entire observation period. A simplified model was then developed and tested, and it was concluded that this model was able to represent the harmonic behaviour of the network.

The next section will deal with testing of the algorithm and demonstrating that the inverter can be used to successfully mitigate low-order harmonics.

4 Hardware-in-the-Loop (HIL) testing

To carry out HIL testing, the PELab was connected to OPAL-RT as described in Section 2 of this report. Initially, static tests were carried out, followed by dynamic tests.

4.1 Static tests

The PELab inverter was initially interfaced to the static model of the Tiverton network, described in Section 3.1. In this model, the loads do not change over time. This approach allows to test the performance of the algorithm under controlled conditions, similar to what was done in WP2. Various static tests were run as part of this analysis, considering different load levels and inverter loading.

Figure 33 shows the three-phase output current of the inverter, before and after harmonic compensation is activated. It is observed that the inverter produces a distorted waveform including various harmonic components. A spike in the current waveform indicates the instant when harmonic mitigation is activated. This transient is due to the fact that the AF functionality is activated by using a switch for testing purposes. In the practice, AF operation is expected to be in service continuously or to be started gradually, and therefore the transient will be much reduced or not present at all.

Figure 34 shows the voltage THD at Tiverton 33 kV busbar (TIVE3) – this quantity has been used through the project to evaluate the effectiveness of the algorithm in improving the system power quality. This figure is obtained for the test conditions shown in Figure 33. However, it is calculated offline from the workspace data, rather than being captured from the oscilloscope. The same script used in the previous work packages is adopted for consistency. One can observe that the voltage THD is reduced when the inverter AF operation is activated (at t = 6 s). The spike in THD calculation corresponds to the switching instant shown in Figure 34.

Figure 33: Current waveform at the inverter terminals (recorded from the oscilloscope).

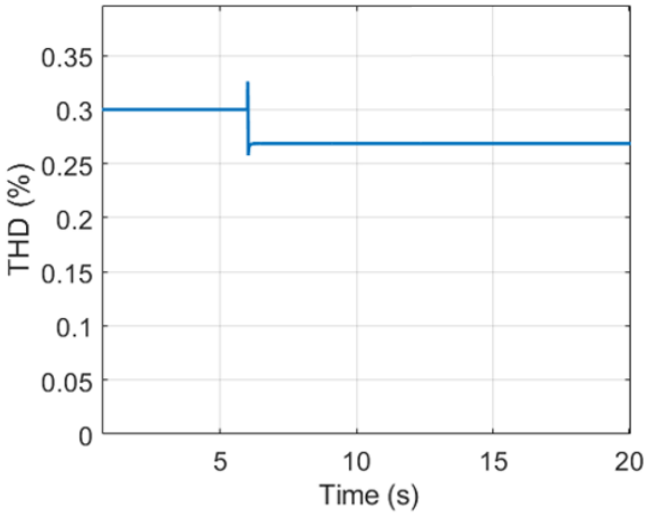


Figure 34: Voltage THD at TIVE3, when harmonic mitigation from the PELab is activated at t = 6 s.

4.2 Dynamic tests

The next part of the HIL tests consisted in connecting the inverter to the complete dynamic model. As already explained in Section 3.3, these tests resulted in instability issues as exemplified in Figure 35 where the test runs normally for approximately half of the observation time (9 days) before becoming unstable and eventually the inverter tripping on overcurrent.

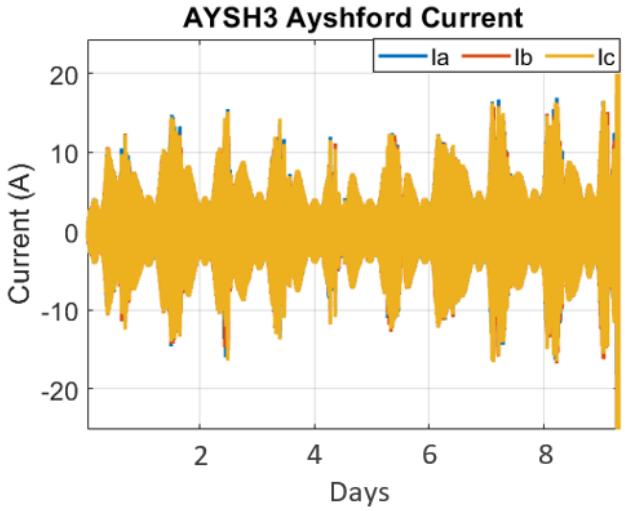


Figure 35: Example of instability observed the initial stages of HIL testing.

When the simplified model with dynamic loads was used, the instabilities disappeared, and tests could be run for the entire observation time.

4.2.1 Shunt resistance

While the tests could be completed for the entire observation period using the simplified dynamic model, high frequency oscillations were initially observed in the THD calculations, as shown in Figure 36a. This behaviour was tracked down to high frequency oscillations in the voltage at TIVE3.

A similar behaviour was previously observed in WP1, and was solved by modifying the shunt resistance connected in parallel to the load models[1].

A similar approach was then tested in WP4, and after a few trials, it was concluded that a shunt resistance with 10 kΩ should be connected in parallel with the dynamic model of the PV farms, as shown in Figure 37. The value chosen is aligned with the ones adopted for the load models. Large values make the model unstable, small values results in current being drawn from the load, so the chosen value is generally chosen based on simulation results, as it is specific on the model under use. The resulting voltage THD is significantly improved and matches closely the results provided in WP2, as shown in Figure 36b.

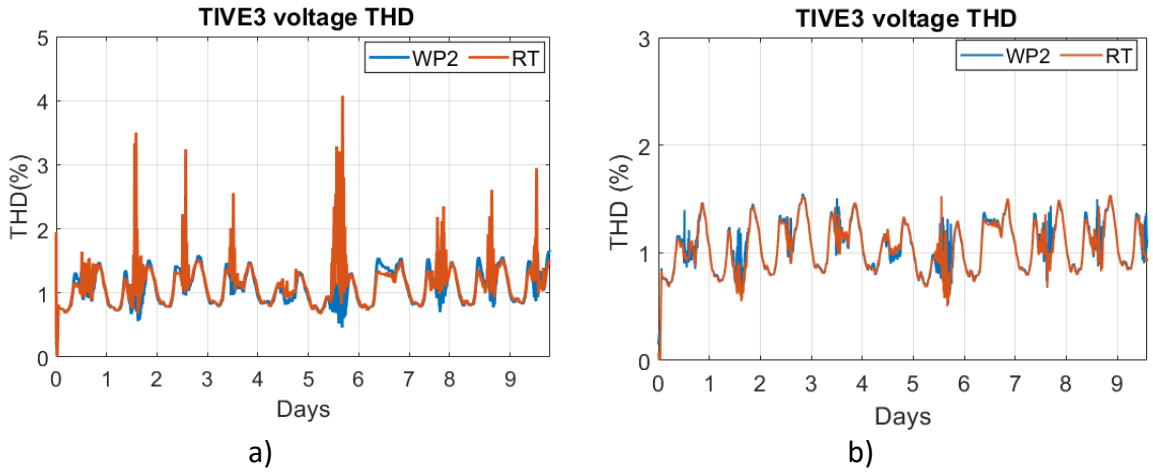


Figure 36: Comparison of voltage THD a) before and b) after adding the shunt resistance in parallel to the equivalent farm models.

[1] From WP1, page 25: A shunt resistance is added in parallel to the dynamic load to allow the numerical solution to converge. This resistance is required because the dynamic load model includes various algorithms to convert the power values to corresponding electrical components, and upon initialisation of the model these electrical components are modelled as open circuits. Therefore, the shunt resistors provide a reference to the ground for the numerical solution to converge. The value of the shunt resistor varies between loads, but it is in the order of 10^4-10^6 Ω to avoid draining large currents from the network.

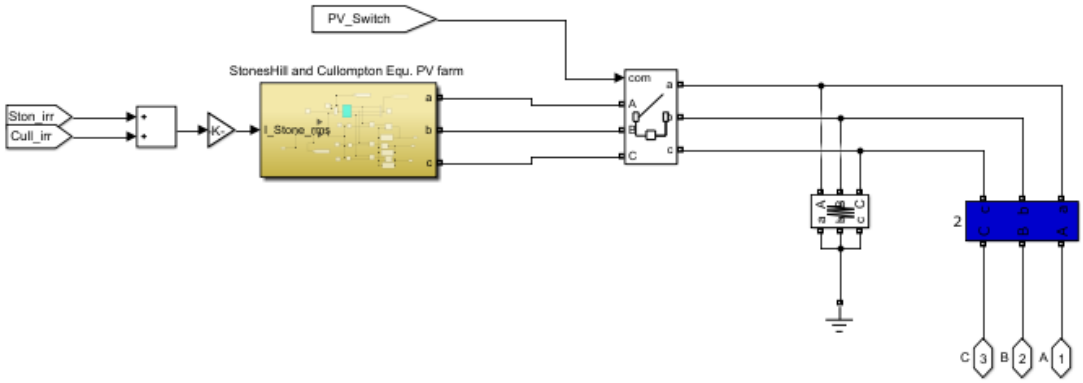


Figure 37: Additional shunt resistance added in parallel to the dynamic PV farm model.

4.2.2 Automatic gain modification

While the addition of the shunt resistance resulted in significant improvement, some further discrepancies were observed when compared to the simulation results, and attention was posed on the automatic gain model, described in detail in WP2 report.

The automatic gain was introduced in WP2 to regulate the fundamental current flow in the inverter. The value of the automatic gain is updated every 10 min to avoid rapid changes in harmonics injection (see WP2 report [3]). Because 100 ms corresponds to 30 min in the time scale used in the model, the averaging time of 10 minutes corresponds to 33.33 ms. This time scale cannot be used in real time, because 0.333 is not an integer of the simulation time, and it was leading to errors in the model. After some tests, the delay was set to 15 min, that corresponds to 50 ms, and it is an integer multiple of 100 µs.

The input current to the automatic gain is the inverter current – this signal needs to be filtered to remove the harmonic components and to ensure that only fundamental current is passed. As a result, the automatic gain includes a filter. In this work package, the filter parameters needed to be adjusted to match the new time step:

- the sampling rate of the filter was changed from 125 kHz (8 µs) to 10 kHz (100 µs)
- the pass band frequency was modified from 40-80 Hz in WP2 to 30-60 Hz.

Results using the most updated version of the automatic gain will be presented in Section 4.3.2.

4.3 Experimental results

The first part of the experimental results shows some screenshots from the oscilloscope, to demonstrate the stable behaviour and the fast response of the inverter. The second part shows results from the workspace, and detailed comparison with WP2.

4.3.1 Results from the oscilloscope

Figure 38-Figure 40 shows experimental results captured with the oscilloscope, when monitoring the measured current.

The top plot within each graph shows a time domain waveform in all cases – the scale is compressed, but it is possible to recognise the times when the inverter is generating current from the solar irradiance. One channel per phase is used.

Figure 38 and Figure 39 shows the results for a case when AF operation is not active. The second plot in both figures shows a zoomed in version of the top plot: Figure 38 indicates a condition when the inverter is operating at night, and very small currents can be detected. Figure 39 shows the case when the inverter is operating during the day and therefore the three-phase currents are more visible.

Figure 38: Inverter current from the oscilloscope when AF operation is not active – the zoomed in window in the second plot shows small current during the night.

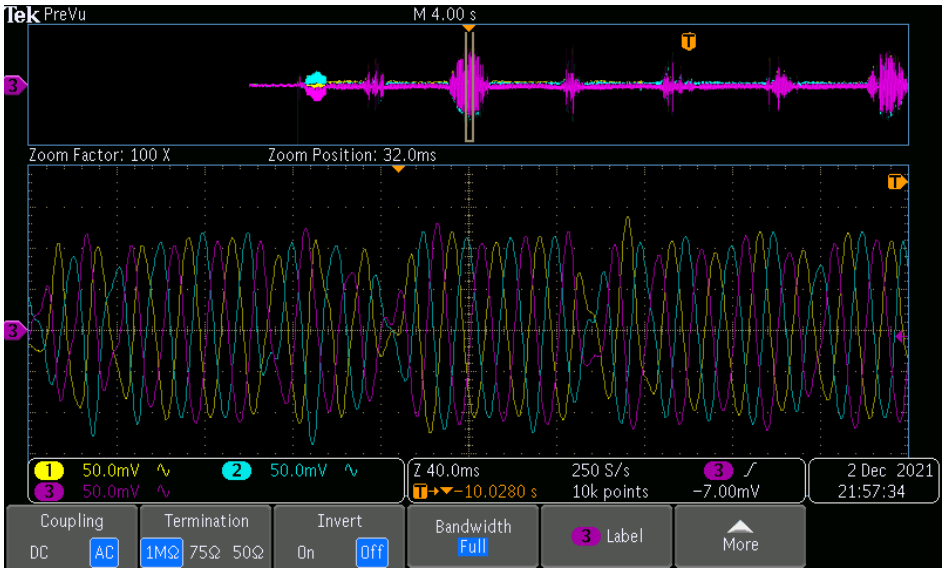


Figure 39: Inverter current from the oscilloscope when AF operation is not active – the zoomed in window in the second plot shows large fundamental current during the night.

Figure 40 shows similar results, but it corresponds to a condition when AF operation is suddenly deactivated: in this case, it is very possible to see in the second graph that there is a noticeable decrease in the harmonic currents injected by the inverter. This test was done to check the robustness of the tests. In the practice, AF operation would be generally always active, and if activated and deactivated, the transition would be implemented more gradually.

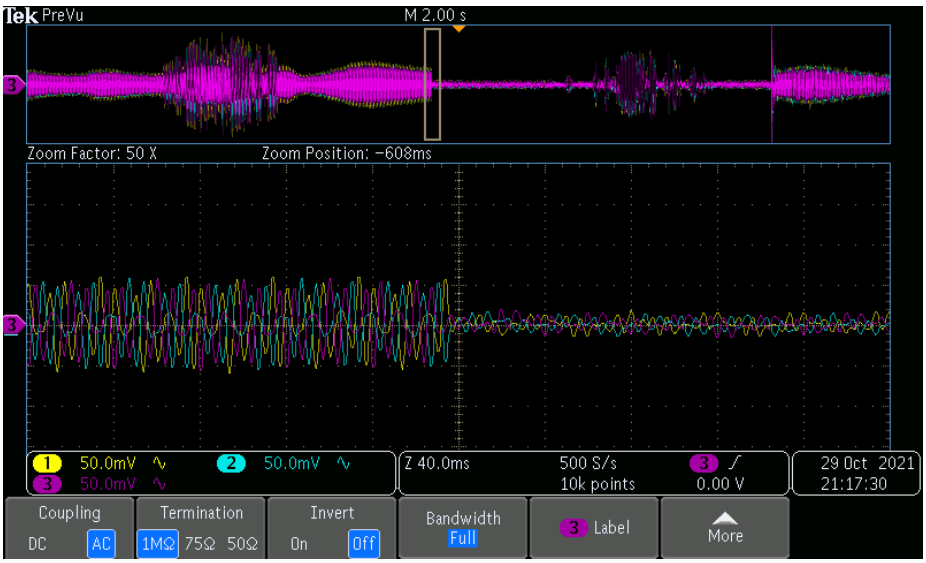
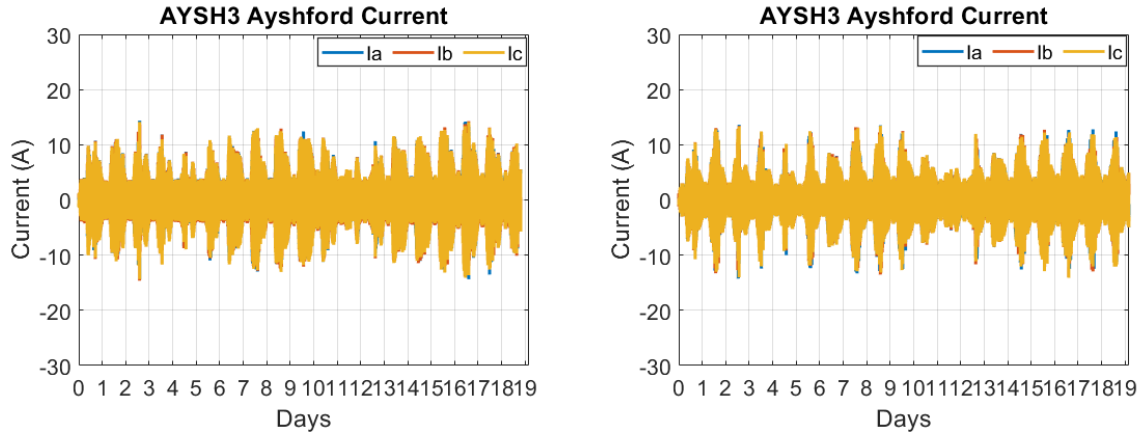


Figure 40: Inverter current, showing the transition between AF operation, and normal operation.

4.3.2 Results from the workspace and comparison with WP2

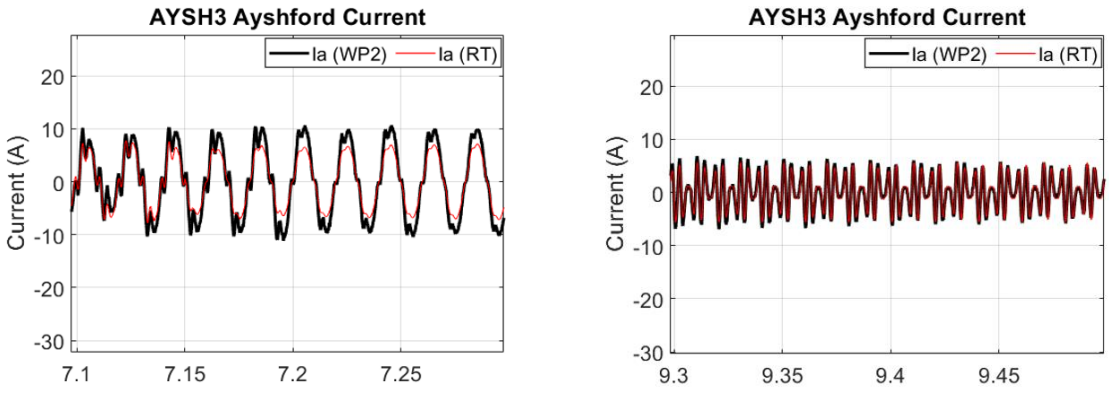
In this subsection, three main quantities will be compared with the results obtained in WP2: inverter current, voltage THD at TIVE3 and transformer losses.

Figure 41 shows the comparison between inverter current obtained in WP2, and in HIL. The variation of the inverter output current is clear, and it is caused by a combination of varying irradiance and varying harmonic injection. The results obtained in WP2 and HIL (WP4) are very close. Figure 42 shows a detailed comparison between phase 'a' current for two sample windows: the first during the daytime and the second during the night. While the trends are very close, during the daytime there is a deviation due to the differences in the automatic gain response. During the night, when the waveform contains mostly harmonics (i.e. the controller acting in compensation mode), the results are closer.



a) WP2 b) HIL

Figure 41: Inverter current with AF operation: a) WP2 results and b) HIL results.



a) b)

Figure 42: Detailed comparison of phase a current during the day (a) and the night (b).

Figure 43 shows the voltage THD obtained from HIL and compared to the results of WP2. One can observe that the two results match very closely. An exact match cannot be expected

due to differences in sampling time, modifications introduced in the PQ data and network reduction. Specifically, one can observe that WP2 results show spikes around midday for day 1 and between day 12 and day 13, that are not present in HIL. These discrepancies were attributed to the different tuning of the automatic gain, and increased sampling time in the HIL tests. These differences prevent the HIL tests to reproduce very rapid variations observed in WP2. However, the results indicate that the performance of the algorithm is very close to the one observed in simulation. A quantitative analysis is provided in Table 2, showing average, minimum and maximum value. These metrics indicate that the match is very close between simulation and HIL tests.

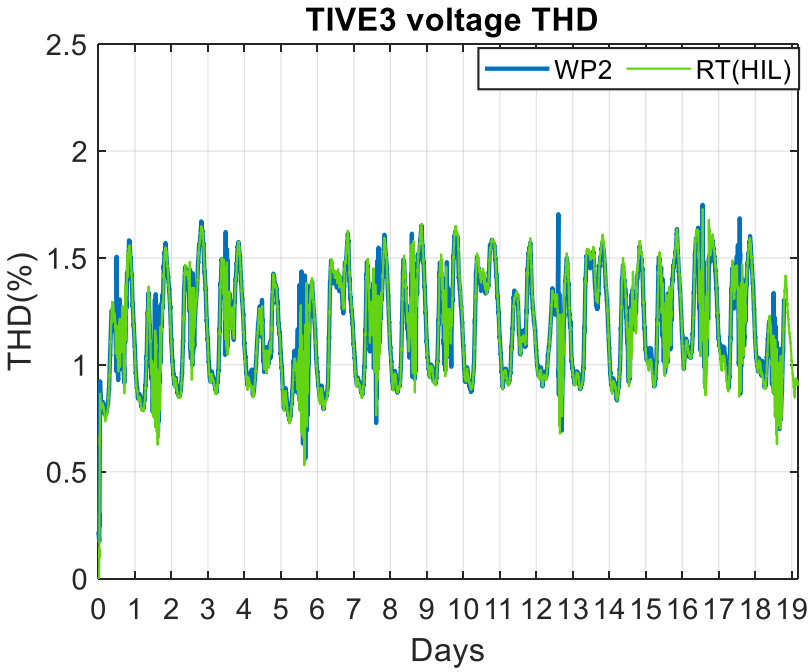


Figure 43: THD at TIVE3 busbar for WP2, and for HIL (with compensation).

Table 2: Comparison of THD for WP2 and HIL (with compensation).

	WP2 (THD) for 19 days (%)	HIL (THD) for 19 days (%)
Mean	1.05	1.05
Max	1.68 @ t=79.3 s (16 d, 13:30 h)	1.67 @ t=79.3 s (16 d, 13:30 h)
Min	0.53 @ t=27.2 s (5 d, 14:00 h)	0.54 @ t=27.2 s (5 d, 14:00 h)

The last quantity considered for comparison is the transformer losses, calculated according to the formulae shown in WP2 report. The comparison between the HIL results and the simulation result is shown in Figure 44. The two curves are very close, thus further reinforcing the consistency of the experimental validation with the results obtained in WP2.

The differences between the two curves are due to the cumulative effect of the changes explained in the previous sections: changes in sampling time, refitting of the PQ data, tuning of the automatic gain. However, overall the trends are very close.

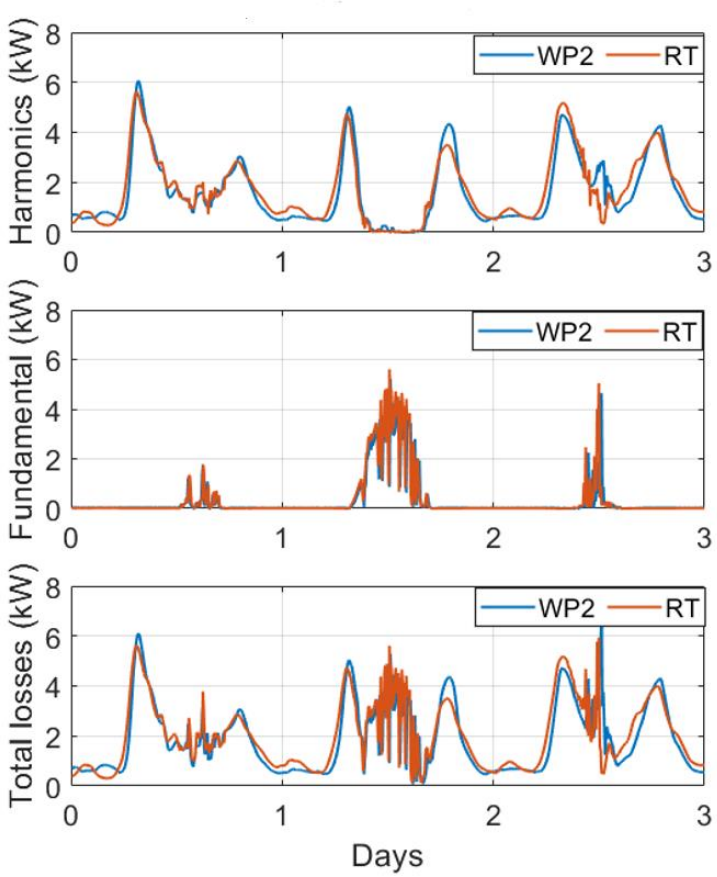


Figure 44: Comparison of transformer losses in a) WP2 and b) HIL. Average loss value: 2.22 kW for HIL and 2.21 kW for WP2.

The rated transformer losses are 5.7 kW, and it can be observed that this value was exceeded a couple of times in Figure 44, both in simulation and in HIL tests. This result is expected as the control algorithm developed in WP2 did not include the implementation of the transformer loss limiter (developed in WP3). However, it can be expected that with transformer loss coefficient included in the model, transformer losses will be kept within the rated value.

4.4 Conclusions

The results presented in this section demonstrate that the experimental results match well the simulation results presented in WP2. Due to limitations in the equipment available, the full network model couldn't be used. However, the use of the simplified model developed still was able to duplicate the harmonic behaviour shown in the previous work packages, and the ability of the developed control system to mitigate harmonics.

5 Lessons learned

The following lessons are learned from this work package:

- The minimum sampling time achievable with the available hardware is 20 µs (while in Simulink 8 µs was used). This limitation may not be specific to the platform used in the project (OPAL-RT 6500) as generally real-time simulations do not allow for small step times to be used. As a result, very short lines included in the Simulink model could not be modelled using distributed parameters, as this representation requires 8 µs sampling time. These lines have therefore been replaced with pi-sections. After adding the control algorithms for the inverters, this sampling time was increased to 100 µs.
- Real-time simulation does not allow using interpolation of PQ data similarly to the Simulink model, as only integer multiples of the time step can be used. This resulted initially in a shifting of the results in RT-LAB compared to simulation. This phenomenon has been corrected by duplicating one point every ten for the high-resolution power quality data. For similar projects involving both simulations and experimental validation, it is recommended to define at the start of the project the requirements on data resolution, to ensure that the same resolution can be used thorough the project.
- Initial HIL tests revealed that the full network model cannot be used as it leads to a high number of overruns and to instabilities. Therefore, it was necessary to develop a simplified network model, that preserved the same harmonic levels as the original model, thus allowing for a straightforward comparison between HIL results and simulation results. The algorithm developed in WP2 can be used for HIL analysis while keeping its structure mostly unaltered. However, some tuning was required due to the differences in the sampling time between Simulink and OPAL-RT. Another major modification is that while in simulation the switching pulses can be generated directly from the reference voltages, in HIL the calculation of the duty cycle is required.

6 Conclusions

This work package dealt with the experimental validation of the harmonic mitigating algorithm developed in this project. To perform this validation, the network model was implemented in an emulator, interfaced with a physical inverter. For the purpose of testing the dynamic behaviour of the algorithm, a simplified network model was used, as the original network model was too large to be executed in real-time.

The equipment available allowed testing the algorithm using only an individual inverter; therefore, the results from this work package have been compared with the ones obtained in WP2. The quantities considered for the comparison are: voltage THD at TIVE3 (the BSP), inverter current and transformer losses. The results of the experimental validation match very closely the simulation results, but some discrepancies have been observed and explained. These differences are caused by the use of a different sampling time in OPAL-RT and in Simulink, by simplification of the network model, and by adjustments required in the measurement data when imported in RT-LAB.

Despite the above limitations, the HIL tests results are very close to the ones obtained in simulation, and they have been quantified by metrics such as average value, peak value and minimum value. The experimental validation confirms that the algorithm developed in this project is effective in reducing harmonics encountered in distribution system, while at the same time the equipment rating is not exceeded. Further validation with the full network model and multiple inverters, thus allowing duplication of the results obtained in WP3 will require the use of more powerful experimental platforms. Additional opportunities for future work are summarised in the next section.

7 Recommendations for future work

This NIA project was proposed as a trailblazer with the aim of assessing the viability of using PV inverters as active filters. The proposed functionality has been tested on both simulation and experimental platforms. Based on the results of this project, various opportunities for further work in this area have been identified:

- HIL tests should be run to include multiple inverters. In this project, HIL testing included one individual inverter due to equipment availability. But a full comparison with the Simulink results would need the use of multiple inverters connected to the grid emulator. This approach will allow carrying out a full comparison with the results obtained in WP3, where various inverters were connected to the network and various feedback measurement points were used.
- The OPAL-RT platform used in this project proved to be inadequate in running the full network model, including the measurement data. Further increase in the sampling time proved not to be practical because it would compromise the accuracy of the control system. More powerful platforms are available to model larger networks and to be interfaced with multiple devices. When testing various inverters, it will be necessary to ensure that the number of inputs and output ports will be sufficient.
- A further step may consist in deploying Power-Hardware-in-the-Loop (PHIL) testing, possibly including a PV panel on the dc side of the power converter. In order to allow power flow through the inverter, power amplifiers will be required to interface the grid emulator to the inverter [4].
- It is recommended to work closely with PV farm developers to gather more data on the PV farms, and specifically on the collector system and the inverter physical configuration and output filters. This will allow testing the algorithm on models that are closer to the real-time operating conditions.
- The ultimate validation of the proposed algorithm will be carried out in the field, however, it is expected that further validation through simulation and experimental tests will be required, working closely with a PV inverter developer or with a PV farm developer.
- In this project, the proposed algorithm has been tested using measurement data from the month of October 2019. It is recommended to collect additional PQ data for summer months (peak PV generation) and winter months (peak demand, and presumably higher harmonic levels). These tests will allow verifying algorithm operation under more extreme operating conditions where the full rating of the inverter may be used for a larger portion of the time.
- Further tuning and validation of the transformer loss coefficient should be carried out in HIL to ensure that the algorithm is effective under varying operating conditions and for different feedback points.

8 Bibliography

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Appendix A: Software in the loop validation with full network model

Initially, the Harmonic Mitigation algorithm was tested in the dynamic model using Software-in-the-Loop (SIL) analysis. In this case, the controller runs on the RT-Lab platform and there is no connection to the external hardware. SIL is an intermediate step that allows verifying operation in real-time using the dynamic model. In this case, the model used in OPAL-RT is very similar to the Simulink model, and no signals are exchanged with the physical inverter. While SIL analysis is very similar to a simulation, it allows testing the model in real time, and therefore it requires a larger time step. This approach allows ensuring that the proposed control still runs with the new time step, and it allows monitoring on the overruns. The SIL results are presented in this appendix as they were used in preparation for HIL tests, that are the subject of this work package.

The results shown in Figure 45- Figure 47 indicates that system operation is as expected, i.e. harmonic compensation works and results in a reduction of voltage harmonic components TIVE3. The average reduction of the main voltage harmonic components (5^{th}, 7^{th}, 11^{th}, and 13^{th}) is approximately 17%, which is comparable to the results obtained in WP2.

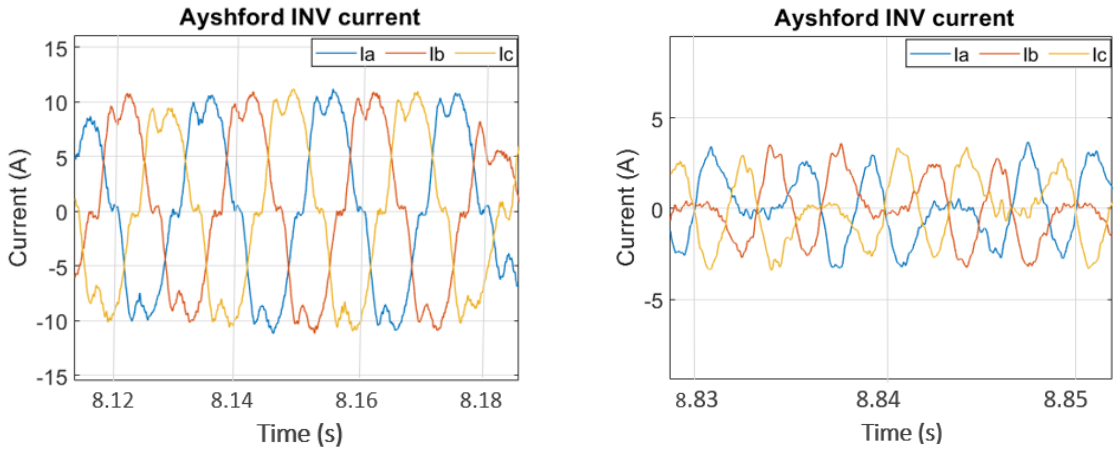

Figure 45: Ayshford inverter current with compensation (SIL).

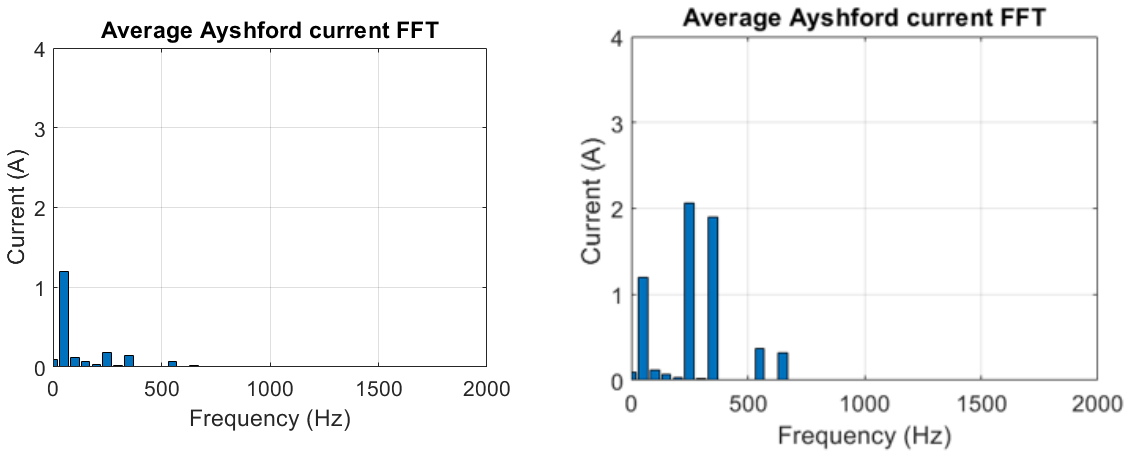

Figure 46: Current FFT with and without harmonic mitigation (SIL).

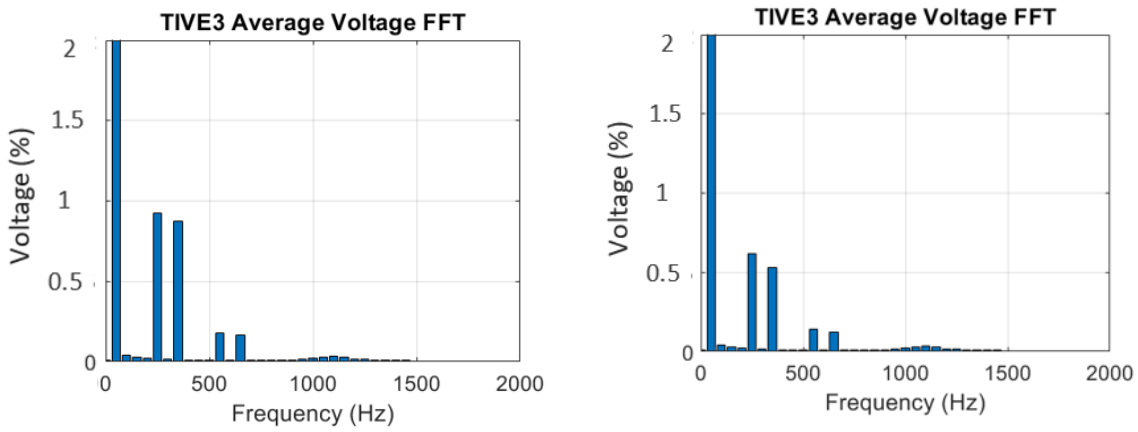

Figure 47: Voltage FFT with and without harmonic mitigation (SIL).